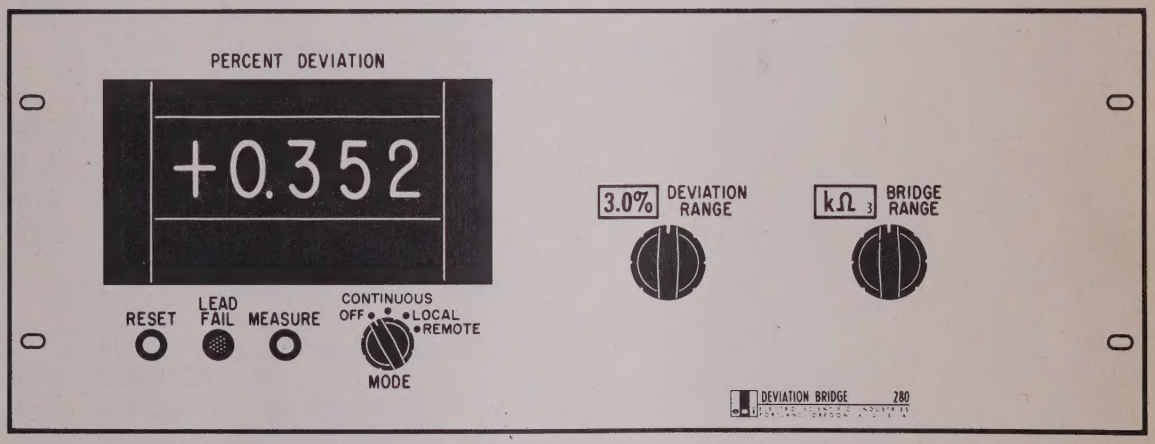
Maintenance Manual
SEPTEMBER 1970

MODEL 280
DEVIATION BRIDGE



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SECTION I

INTRODUCTION

1.1 DESCRIPTION

The ESI Model 280 Deviation Bridge is a fully automatic Kelvin bridge which measures and displays digitally the percent deviation of the unknown from the setting of the standard, times a multiplier. It has a programed generator, a null detector with programed sensitivity, and digital controls. The instrument provides three linear deviation ranges: 30%, 3%, and 0.3% and five bridge ranges from one kilohm to 10 megohms full scale, all manually selected on the front panel. The Model 280 also provides:

Automatic connection verification to stop the system if the unknown is not connected. Lead failure is indicated by a light on the front panel.

Good 60 Hz rejection.

Automatic zeroing to cancel thermal emf in bridge and unknown and amplifier drift in generator and detector.

Low power in unknown to minimize self-heating.

Power limiting to prevent damage in bridge.

High measurement speed - 100 milliseconds or less.

Overload light on display to indicate detector saturation, generator current limiting or out-of-range deviation.

All information and remote controls available at rear panel for connection to auxiliary equipment.

Independent grounds in measurement and logic sections for clean digital signals and accurate measurements.

1.2 SPECIFICATIONS

1.2.1 Electrical Specifications

Resistance accuracy

Initial: ±(50 ppm of reading + 0.2 of least step).

Long Term: ±(100 ppm of reading + 0.5 of least step).

Power in Unknown: Less than 10 milliwatts, if the unknown resistor is within ±30% of the setting.

Measurement Speed: Less than 100 milliseconds per measurement.

Deviation Ranges: 30%, 3% and 0.3%. (Maximum deviation readout ±2999 and then overload is indicated.)

Deviation Accuracy: ±(0.1% of reading + least significant digit) over all ranges.

Deviation Range	Deviation Resolution	Usable Resistance Range* for Calibrated Deviation
± 0.3%	1 ppm	10 Ω up to 1.111110 megohms
± 3.0%	10 ppm	1 Ω to 11.11110 megohms
± 30%	100 ppm	0.1 Ω to 11.11110 megohms

*Outside these ranges the deviation reading is no longer calibrated.

Voltage Across Unknown Resistors: Equals value given in table below times (1 + Δ) where Δ is resistor deviation from bridge setting.

Full Scale Resistance Ranges

Deviation Range	1k	10k	100k	1M	10M
0.3%	0.25V	2.5V	7.91V	25V	25V
3.0%	0.079V	0.791V	2.5V	7.91V	25V
30%	0.025V	0.25V	0.791V	2.5V	25V

Temperature Coeffecient: Less than ±(10 ppm of reading + 1/10 of least step) per °C.

Thermal EMF Cancellation: Accomplished by auto zero circuitry up to approximately ±0.5 millivolt of emf.

Detector Zero: Automatic.

Normal Mode AC Rejection: Greater than 80 dB at 60 Hz (50 Hz for units modified for 50 Hz). (Greater than 60 dB at 60 Hz ±0.1%. If 60 Hz pickup is high enough to cause incorrect readings, an overload will be indicated.)

Digital Interface Configuration: 1248 BCD for the deviation readout (specify 1-state positive or negative). 10-line coded switch closures for range indication and the decades. "Remote start" and "conversion complete" signals available at the connector.

External Leads: Bridge error is increased 1 ppm per 10 milliohms of lead resistance connected to UNKNOWN terminal 2. Lead resistance on UNKNOWN terminals 3 and 4 should not be higher than that on 2.

Lead Check: Each time a measure signal is given to the bridge, the unknown leads are checked for continuity. If the sum of the resistance of the leads attached to UNKNOWN terminals 1 and 2, or to 3 and 4, is greater than 2 Ω (±1/2Ω), the LEAD FAIL light will turn on and the measurement will not proceed.

Power Limit: Bridge generator voltage is regulated and current limited to prevent greater than 3/4 watt in bridge.

Power Requirement: 117 VAC, 60 Hz, 40 watts. Unit can be modified for 220 VAC, or 50 Hz operation.

1.2.2 Physical Specifications

Dimensions: Height 7.0 in. (17.8 cm), width 19.0 in. (48.3 cm), depth 16.25 in. (41.3 cm).

Weight: 39 lb (17.69 kg).

SECTION II

CONTROLS AND CONNECTORS

2.1 FRONT PANEL CONTROLS AND INDICATORS

Figure 2-1 shows the controls and indicators on the front panel of the bridge.

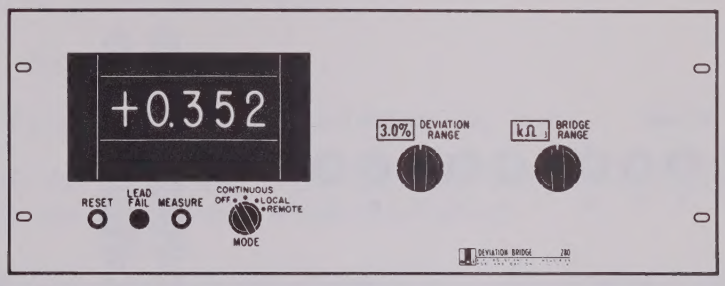


Figure 2-1. Model 280 Controls and Indicators

MODE switch selects the manner in which the test is run. In LOCAL position, the instrument makes one measurement each time the MEASURE pushbutton is pressed. In the CONTINUOUS position, the instrument performs a measurement approximately every 70 to 90 milliseconds. If CONTINUOUS MODE is being used, always push the RESET button before resistors are changed. In REMOTE position, the instrument accepts remote control measurement start signals.

MEASURE pushbutton: In CONTINUOUS MODE, starts a series of measurements which continue until RESET is pressed or MODE is changed.

In LOCAL and REMOTE MODE, initiates a single measurement cycle at the end of which the bridge returns to reset condition.

RESET pushbutton stops the measurement cycle. It is used to set all functions to the initial state. In CONTINUOUS MODE it stops the measurement series.

LEAD FAIL lamp indicates lack of connection to the unknown. When this lamp is lit the system is automatically stopped, and the RESET pushbutton must be pressed before measurements can be made again. In CONTINUOUS MODE the lead check is bypassed after the first measurement.

DEVIATION RANGE switch selects the desired deviation range, ±0.2999% full scale to ±29.99% full scale in three ranges full scale. The window shows the approximate maximum deviation.

BRIDGE RANGE switch selects the bridge range, 1111.1110 ohms to 11.111110 megohms full scale in 5 ranges. The window shows the units to be read with the RS 727 Resistance Standard setting.

PERCENT DEVIATION numerical display indicates the deviation of the unknown resistor from the system setting in percent of the system setting. An overload light indicates detector saturation, generator current limiting, or out-of-range deviation. A plus sign indicates that the unknown resistance is higher than the system setting. Plus and minus signs remain correct even when the overload light is on.

2.2 REAR PANEL CONNECTORS

Figure 2-2 shows the connectors on and to the rear panel of the bridge.

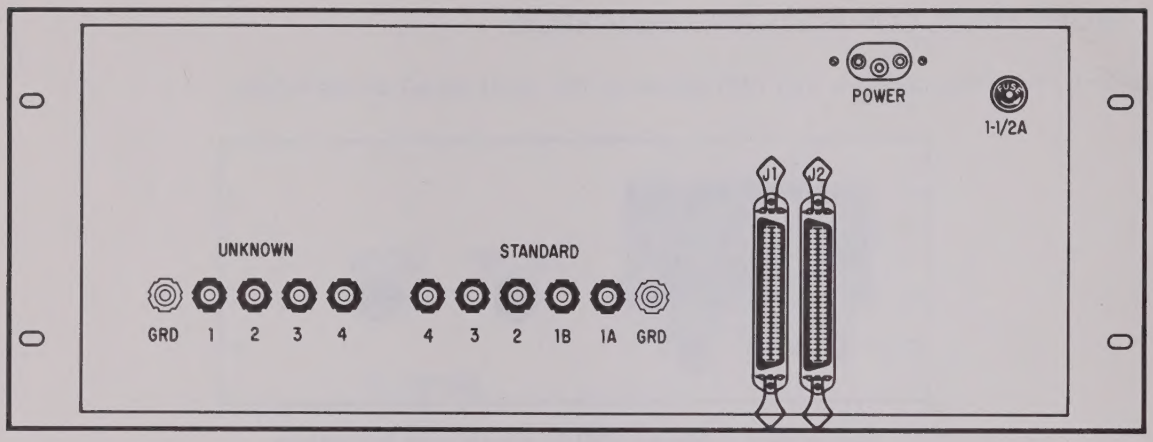


Figure 2-2. Model 280 Rear Panel Connectors

STANDARD terminals 4 3 2 1B 1A GRD connect to respective terminals, with corresponding number, on the rear panel of the standard.

UNKNOWN terminals GRD 1 2 3 4 connect to unknown resistor(s) by means of supplied connection assembly and Kelvin Klips or by shielded test leads.

POWER socket at upper right connects to line voltage by means of the power cord supplied with the instrument.

FUSE socket holds a 117 V, 1-1/2 A line fuse.

Jack 1 (J1) connects a cable to auxiliary equipment.

Jack 2 (J2) connects a cable of four wires to J3 of the Resistance Standard.

SECTION III

ALIGNMENT

3.1 ALIGNMENT VERIFICATION

Those parts of the Model 280 which are adjustable by internal trimmers are listed as follows:

Logic Section: 300 Hz Oscillator Frequency

Generator Section: Voltage and Current

Detector Section: Zero, Plus Full Scale, and Minus Full Scale

It is possible to verify that the settings of all Model 280 trimmers are acceptable without opening the instrument. Alignment verification is described below.

1. The 300 Hz oscillator is used to time the operation of the mercury-wetted latching relays which connect the lead check circuit to appropriate points. If the frequency of the oscillator is low, the lead check may take a few milliseconds longer than the normal 13 milliseconds, but there will not be any other effect. If the frequency is too high, the lead check will not work reliably. Therefore, if the Model 280 is indicating failures correctly (a matter that can be checked by purposely opening the leads), and the measurements are proceeding in a normal fashion and a normal amount of time, it is correct to assume that the 300 Hz oscillator does not need alignment.

2. The detector zero is not likely to drift, and it is possible that it may never need trimming. If, however, the detector zero adjustment is not set correctly, all deviation indications, independent of the deviation range, will be incorrect by the same number of digits. Therefore, if changing the DEVIATION RANGE from 0.3% to 3% to 30% results in the same indication of percent deviation each time (±one significant digit), the detector zero does not need alignment. For example, if readings for the same resistor on the three deviation ranges are -.2977%, -0.297%, and -00.30%, a zero adjustment is not needed. To change the zero by one least significant digit, it takes a change of one millivolt in the offset of the most sensitive stage of the detector that can cause a change in the zero.

3. The settings of the generator voltage and detector sensitivity trimmers may be checked by making a known percentage change in the value of an unknown resistor and observing if the deviation display indicates the correct change. Observing changes is important because actual readings are affected by the accuracy of the bridge and the accuracy of the unknown resistor. A 0.02% resistance decade box is a convenient "unknown" to use for this test. Any or all of the resistance and deviation ranges may be used. It is desirable to observe the change between two readings that are near zero deviation and full-scale deviation, both on the same side of zero. By completely separating the plus and minus deviation changes, the effects of the two detector adjustments may be observed separately. If the two readings are on opposite sides of zero, the display will probably drop one least significant digit.

   The generator voltage alignment affects plus and minus deviations equally. If it is out of adjustment, both plus and minus deviations will be too large or too small. The detector plus full-scale alignment will affect only plus deviation readings and the detector minus full-scale alignment, only minus readings. Therefore, if both plus and minus deviation

changes are correct (±0.1%) it is very unlikely that generator voltage and detector sensitivity trimmers have drifted. It is unlikely that all three would change by the same amount and in the proper directions.

4. The generator current alignment affects the point at which the generator crosses over from voltage regulation to current limiting in order to protect the bridge and cause the display to indicate an overload. If the Model 280 will read a 9.8 Ω resistor on BRIDGE RANGE Ω_1 and DEVIATION RANGE 0.3% without an overload indication, the generator current trimmer does not need attention.

3.2 EQUIPMENT REQUIRED

Minimum use specifications will aid in the selection of alternate equipment. Be sure alternate items meet the requirements.

Item	Minimum Use Specifications	Test	Recommended Equipment
Decade Resistor	Range: 0.1 Ω to 12 MΩ, 0.02%	Deviation Alignment, Detector Plus and Minus Full-scale Alignments	ESI Model DB 877
Digital Voltmeter	Integrate ≈17 ms	Voltage Alignment	Datatech Model DVX-315
Oscilloscope	Can measure period and amplitude of 300 Hz square waves	300 Hz Oscillator Alignment	Almost any

NOTE

This procedure assumes that the Model 280 is connected to a Model RS 727 Resistance Standard.

3.3 ALIGNMENT PROCEDURE

3.3.1 300 Hz Oscillator Frequency Alignment

1. Connect the input of the oscilloscope to Pin 17 of the frequency source board.

   The chassis of the oscilloscope and the Model 280 should be connected through the power line ground. Be sure the logic ground of the Model 280 is tied to the chassis ground.

2. Set oscilloscope sensitivity to approximately 2 V per cm.
3. Adjust the trimmer on the frequency source board so that the period of the observed square waves is between 3.2 and 3.4 ms.

3.3.2 Generator Voltage Alignment

1. Using BRIDGE RANGE Ω_1 and DEVIATION RANGE 0.3%, set Model RS 727 to measure a 1 kΩ resistor.

   Balance the bridge so that the deviation reading is on scale.

2. Connect DVM input between STANDARD terminals 2 and 3.

   Do not ground either input. Ignore the deviation reading.

3. Set Model 280 MODE switch to CONTINUOUS.
4. With DVM reading continuously, observe greatest plus and minus readings.

   Greatest readings should occur when Model 280 generator does not reverse polarity during the sampling period.

5. Adjust generator voltage trimmer so that the difference between the greatest plus and minus readings is 50 V ± 20 mV.

   After adjustment both readings should be between 24.9 V and 25.1 V.

3.3.3 Generator Current Alignment

1. Using BRIDGE RANGE Ω_1 and DEVIATION RANGE 0.3% measure the 10 Ω setting of the decade resistor. Balance Model RS 727 for minimum possible deviation.

   Model 280 will balance at a setting greater than 10 ohms due to decade resistor zero resistance. Be sure overload light is not on when balance is completed.

2. Reduce decade resistor and Model 280 settings by one ohm each.

   The decade resistor should now be set to 9 ohms.

3. With Model 280 measuring continuously, adjust generator current trimmer so that a small motion of it will cause overload lamp to be lit continuously.

   Correct setting is just on the verge of overload, but not overloaded.

3.3.4 Detector Zero Alignment

1. Using BRIDGE RANGE kΩ3 and DEVIATION RANGE 3%, measure the 100 kΩ setting of the decade resistor. Adjust Model RS 727 for deviation reading of -0.050.
2. Change Model 280 DEVIATION RANGE setting to 30%.
3. Adjust detector zero trimmer so that deviation reading is -00.05. Repeat steps 1 through 3 until no adjustment is needed.

3.3.5 Detector Plus Full-Scale Alignment

1. Using RESISTANCE RANGE kΩ3 and DEVIATION RANGE 3%, measure the 100,000.0 ohm setting of the decade resistor. Adjust the setting of the Model 280 so that the deviation reading is + 0.010%. Use the CONTINUOUS MODE.
2. Change the setting of the decade resistor to 103,000.0 ohms.
3. Adjust the detector plus full-scale trimmer so that the deviation reading is + 3.010%. Ignore the overload indication.

3.3.6 Detector Minus Full-Scale Alignment

1. Using RESISTANCE RANGE kΩ3 and DEVIATION RANGE 3%, measure the 99,999.X ohm setting of the decade resistor. Adjust the setting of Model 280 so that the deviation reading is -0.010%. Use the CONTINUOUS MODE.
2. Change the setting of the decade resistor to 96,999.X ohms.
3. Adjust the detector minus full-scale trimmer so that the deviation reading is -3.010%. Ignore the overload indication.

NOTE

There are five additional trimmers inside Model 280's with serial numbers 033001 and after located at the top of the instrument near the front panel. These trimmers adjust the full-scale accuracy of each range of the Model 501 System. They should not be adjusted at this time. Instructions for these trimmers are in the Model 501 Calibration Procedure.

SECTION IV

THEORY

The Model 280 bridge makes a precision comparison between an unknown resistor and a standard resistance value. The resulting difference is displayed as the deviation of the unknown from the setting, in percent of the setting.

The usual sources of error in such measurements have been considered and the system has been designed to avoid them.

4.1 BRIDGE CIRCUIT

A four-terminal, Kelvin comparison bridge has been used for the circuit. The Kelvin circuit minimizes errors from lead and connection resistances. This is accomplished by making two connections to each end of the unknown resistor. Lead and connection resistances are placed either in generator leads where they will have no effect, in series with high value internal bridge arms where they will have an insignificant effect, or in series with the bridge yoke shunt where their effect can be eliminated by the proper yoke ratio.

4.2 GUARDING

The bridge is guarded so that high resistance leakage paths for both the unknown and standard resistors are intercepted. The chassis is used as the guard shield. Leakage resistances are shunted across low resistance internal bridge arms or the detector. Guarding of a three-terminal unknown resistor can be accomplished by connecting the bridge chassis to its leakage intercept terminal. This guarding permits accurate measurement of high value resistors even in humid environments. The guarding has been extended into the bridge detector and lead check circuits as well as the switch and connector mountings.

4.3 MEASUREMENT SEQUENCE

The measurement sequence has been programed to make a precision measurement quickly.

4.3.1 Preconditioning

Resistors do not exhibit a constant resistance value instantly because of associated inductances and capacitances. A short pre-conditioning time is necessary to permit transients to die out. Constant current is supplied to the unknown resistor for 1/60 second before any measurement is made. (1/50, 3/60 or 3/50 can also be provided by internal changes. This circuit change will change all periods referred to as 1/60 second.)

4.3.2 Deviation Measurement

The deviation of the unknown resistance from the standard setting is measured by placing a known value of voltage across the standard resistor and measuring the difference between the value of voltage across the unknown resistor and the value it should be if the unknown was its indicated value. By controlling the Kelvin bridge supply voltage to give the proper fixed voltage across the standard, the conventional detector signal is proportional to the desired deviation. The detector sensitivity can then be adjusted to read deviation directly in percent of the set value of resistance. The supply voltage is controlled by a solid state circuit which maintains a predetermined, fixed voltage across the standard resistor. The detector gain is fixed and controlled by a solid state operational amplifier. The stability of these circuits assures accuracy of the four-digit percent deviation reading.

4.3.3 Detector

The detector signal is read by a dual-slope integrating digital voltmeter. To avoid the effects of fixed error voltages, which may occur in the generator, the bridge itself, and the detector, two measurements are made and the results added. For the second measurement the bridge generator voltage and the detector polarity are both reversed. Any fixed error voltage (for example, a residual output from the generator when it is thought to be off, thermal emf's in the bridge components, or a non-zero detector reading without a signal to the detector) would increase one measurement and decrease the other by an equal amount thus cancelling its effect. The integration is done for 1/60 second intervals for both measurements. Any error signal of 60 Hz, or any integral multiple of 60 Hz, will integrate to zero each 1/60 second. Thus hum pick-up effects are avoided. Error signals of other frequencies are also attenuated by the integration technique but they are not completely eliminated. Both series and induction motors produce signals different from 60 Hz and its harmonics. These signals may cause trouble if such motors are used near the measurement system.

4.3.4 Deviation Display

The display reading is generated by counting a high frequency signal while the stored integrator signal is removed by integrating at a constant rate in the other direction. When the integrator signal reaches zero the counter reading is transferred to the display panel.

4.4 LEAD CHECK

Disconnected or high-resistance leads to the unknown resistor can cause serious measurement errors. A lead checking bridge checks the series resistance of the leads to each end of the unknown resistor. If a high resistance is found in any of the four leads the measurement cycle is stopped and the LEAD FAIL light is turned on. When the leads are properly attached the measurement cycle continues. Three modes, local, remote, and continuous are provided. In the LOCAL MODE each measurement must be initiated by pressing the measurement button on the front panel. In REMOTE MODE the bridge can still be operated from the panel but MEASURE, RESET and some other control functions are made available externally. In CONTINUOUS MODE, measurements are made in sequence, starting when the MEASURE button is pushed and continuing until the RESET button is pushed. In CONTINUOUS MODE the leads are tested only once. If they fail during the series of measurements, the bridge answers may be wrong.

4.5 CIRCUITS AND TIMING

The bridge diagram is shown in Figure 4-1 and the time sequence of signals and events is shown in Figure 4-2.

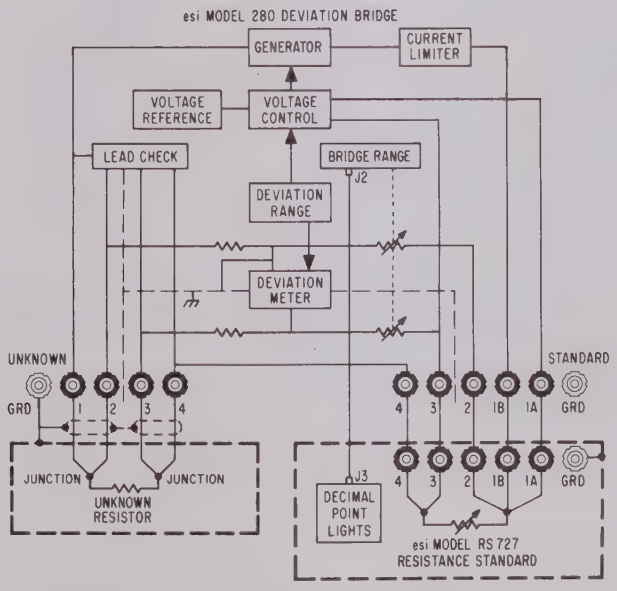


Figure 4-1. Deviation Measurement Diagram

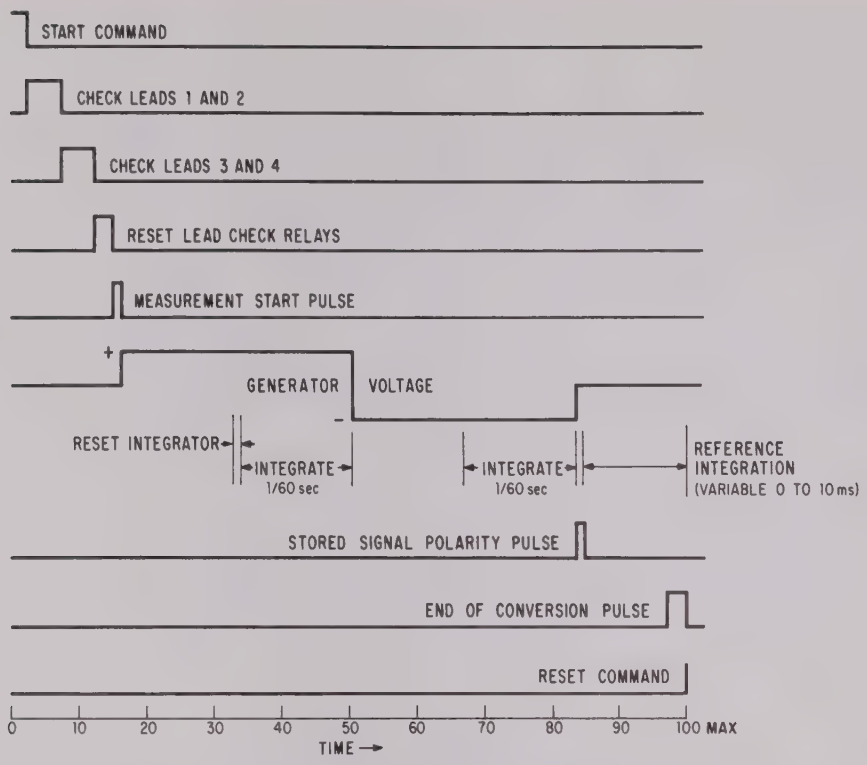


Figure 4-2. Time Sequence of Signals and Events

4.6 REMOTE CONNECTIONS

Digital logic circuits are provided for remote indication and control so that the system can be made a part of larger measurement or automatic adjustment systems.

SECTION V

TROUBLESHOOTING

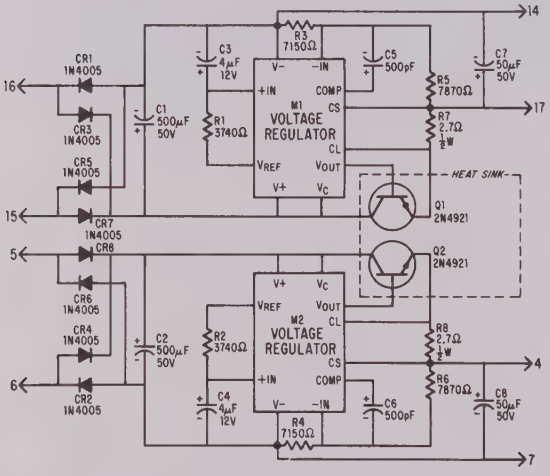
The following functional descriptions are intended as an aid to troubleshooting. In most areas of operation possible problems, in terms of the circuit or component likely to be responsible, are identified in the section describing that circuit. The logic of the Model 280 is treated separately from the rest of the instrument.

5.1 CIRCUIT ASSEMBLIES AND CHASSIS-MOUNTED COMPONENTS

5.1.1 15-Volt Regulator

ESI Part No. 19875

NOTE: REFERENCE DESIGNATIONS OF COMPONENTS IN ASSEMBLIES AND SUBASSEMBLIES ARE ABBREVIATED FOR CLARITY. PREFIX DESIGNATION WITH DESIGNATION OF ASSEMBLY WHEN REFERING TO COMPONENT OUT OF CONTEXT. FOR EXAMPLE, C1 IN ASSEMBLY A1 SHOULD BE A1C1, R2 IN ASSEMBLY A2 SHOULD BE A2R2, SUBASSEMBLY A1 IN ASSEMBLY A2 SHOULD BE A2A1, AND R3 IN THAT SUBASSEMBLY SHOULD BE A2A1R3



A1A3, A2A2, A3A11

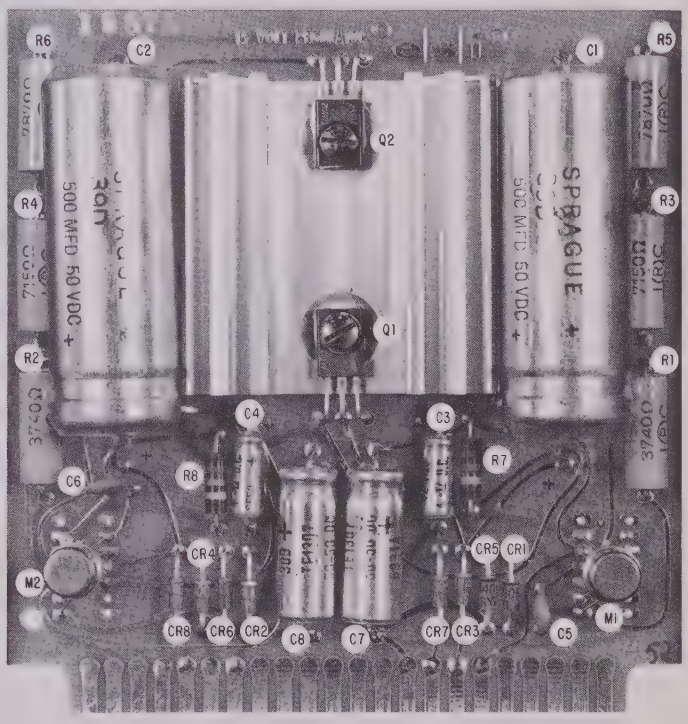


Figure 5-1. 15-Volt Regulator Assembly (19875)

This assembly has two identical 15-volt regulators. Since each regulator is supplied from a separate transformer winding, either side of the output of each circuit may be connected to ground, the outputs may be floated, or connected in series to make a 30-volt source. The plus side of one circuit and the minus side of the other are tied to ground, making a ±15-volt source to supply power for operational amplifiers.

Because the two circuits are identical, only one of them will be detailed here. The source of the unregulated ac voltage, the transformer winding, connects to the circuit on Pins 15 and 16. (Pins 5 and 6 for the other circuit). The plus side of the regulated dc output connects to Pin 17 (Pin 4 for the other circuit). The minus side of the regulated dc output connects to Pin 14 (Pin 7 for the other circuit).

Diodes CR1, CR3, CR5, and CR7 rectify the unregulated ac voltage.

Capacitor C1 filters the rectified ac voltage. The unregulated dc voltage on capacitor C1 is the source of current for the output of the circuit and also is used to operate the integrated circuit voltage regulator M1. The value of the unregulated dc voltage, depending on line voltage, is approximately 20 to 25 volts.

The integrated circuit voltage regulator M1 has a voltage reference, an error amplifier, a series pass transistor and provision for current limiting. An addition series pass transistor Q1 is used in the 15-volt regulator because the transistor internal to the integrated circuit does not have sufficient current or power capability.

Capacitor C3 filters the internal voltage reference of M1 and reduces the noise in the output. If C3 has low internal resistance, the output of the 15-volt regulator circuit will be low.

Resistors R3 and R5 set the output voltage. If the value of R3 were raised, the output of the circuit would be higher. If the value of R5 were raised, the output of the circuit would be lower.

Resistor R1 reduces drifts in the output of the 15-volt regulator caused by changing bias currents in M1. Errors in the value of R1 will probably have small effect on the value of the output voltage.

Capacitor C5 stabilizes the error amplifier in M1. If C5 were faulty, it could cause errors in the output voltage or circuit oscillating.

Resistor R7 sets the current limiting level of the output. When the voltage drop across R7 increases to approximately 0.65 volts, the output will current limit.

Capacitor C7 is the final output filter. An open capacitor could cause excessive output noise or ripple. A capacitor with low internal resistance could reduce current available to the load. The voltage on C7 should be between 14 and 16 volts, and should have less than 100 millivolts peak-to-peak ripple.

5.1.2 Detector Preamplifier Assembly

ESI Part No. 20892

This assembly has the first stage of gain in the detector section of the Model 280. (See Figure 5-2). It has a ±15-volt regulator, a low noise FET operational amplifier AR1, gain-setting resistors R1 to R8, voltage-limiting diodes CR7 to CR10, and a high-frequency roll-off capacitor C7.

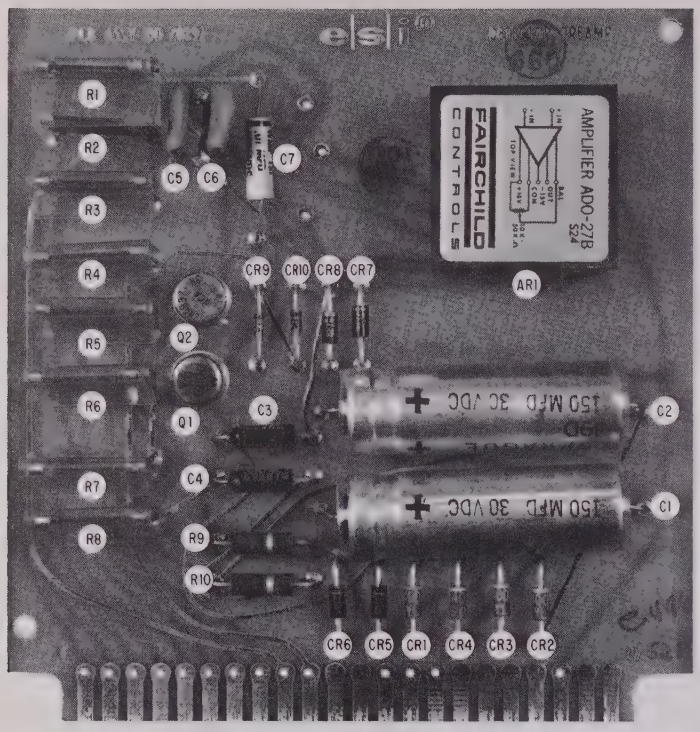
The assembly has its own ±15-volt regulator, to decouple the preamplifier from the rest of the detector. This reduces noise in the preamplifier and the possibility of high-frequency oscillations.

The source of the unregulated ac voltage, the center-tapped transformer winding, connects to the circuit on Pins P, R and S.

Diodes CR1 to CR4 rectify the unregulated ac voltage.

Capacitors C1 and C2 filter the rectified ac voltage. The value of the unregulated dc voltage on the capacitors, depending on line voltage, is approximately 20 to 25 volts.

Resistors R9 and R10 supply the current for voltage reference diodes CR5 and CR6.



CAUTION

Use caution when probing around this circuit. The supplies are not current-limited and an inadvertent momentary short could cause the transistors to fail.

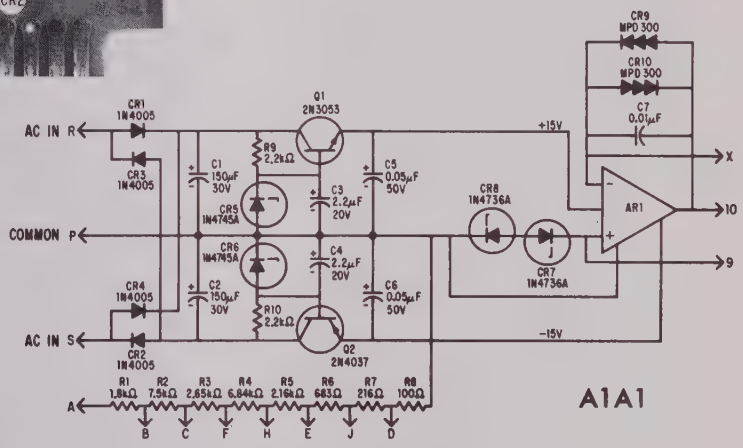


Figure 5-2. Detector Preamplifier Assembly (20892)

Capacitors C3 and C4 filter the reference voltages. The dc voltages on the capacitors should be between 15 and 17 volts.

Transistors Q1 and Q2 are the series pass transistors. They are connected as emitter followers and should have an emitter-to-base voltage of about 0.7 volts. If the outputs of the ±15-volt regulators are too high, it is probably caused by emitter-to-collector shorts in the transistors.

Capacitors C5 and C6 are high-frequency decoupling capacitors.

The high side of the Model 280 bridge output signal connects to Pin 9 of the detector preamplifier. In a normal Model 280 operating with detector instead of the unknown grounded, the low side of the detector output is grounded and is tied to Pin P, the detector guard box, and chassis ground.

The output of the detector preamplifier is Pin 10 and is connected to the input of the next detector stage, the detector assembly.

The diodes CR7 and CR8 protect the detector preamplifier from excessive input voltages resulting from large bridge outputs or voltages inadvertently connected to the unknown resistor. Faulty diodes could result in non-linear bridge deviation readings.

AR1 is a low-noise, high-gain FET input operational amplifier. It is connected as a non-inverting amplifier with the gain determined by resistors R1 and R8. To assist in quick overload recovery, the output of the amplifier is limited to approximately ±2 volts by diodes CR9 and CR10. Capacitor C7 reduces high-frequency noise in the amplifier output. A faulty diode or capacitor could result in non-linear bridge deviation readings.

The amplifier AR1 does not have a zero control because any offsets in its input will be cancelled out in the auto-zeroing procedure of the Model 280. However, if the amplifier offset were excessive, it could cause the Model 280 to indicate an overload (Ⓛ) before readings of ±2999% were reached on those ranges where the detector preamplifier gain is high. This problem might also be caused by excessive 60 Hz pickup in the bridge. Use an oscilloscope on the test points on the detector assembly (ESI Part No. 20890) to observe the waveform of the voltage before making a decision. (See the following description of the detector assembly circuit.)

The gains of the detector preamplifier are given in the table below. The voltage at Pin 10 equals the voltage at Pin 9 plus the offset voltage of AR1 times the gain:

$$V\ 10 = (V\ 9 + \text{Offset})\ \text{Gain}$$

The offset voltage of AR1 should be between -0.3 and +0.3 millivolts.

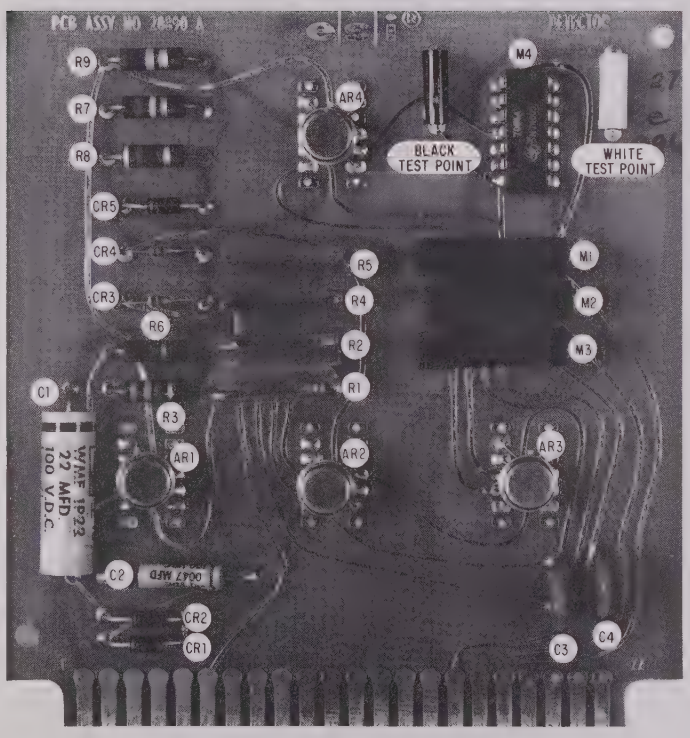
DEVIATION RANGE	BRIDGE RANGE 1	2	3	4	5
0.3%	202	22	12.649	22	202
3%	63.878	6.957	4	6.957	20.2
30%	20.2	2.2	1.2649	2.2	2.02

Table 5-1. Detector Preamplifier Voltage Gains

If the bridge will not deviate far enough only on those ranges that have high detector preamplifier gain, the problem may be due to low open-circuit gain in the operational amplifier AR1. Excessive noise (more than 2 or 3 least significant digits) on BRIDGE RANGE Ω_1 and DEVIATION RANGE 0.3% may be due to excessive noise in operational amplifier AR1. On those ranges with the highest detector preamplifier gain (202) one least significant digit is equivalent to a 1/2-microvolt signal at the input of the detector preamplifier.

5.1.3 Detector Assembly

ESI Part No. 20890



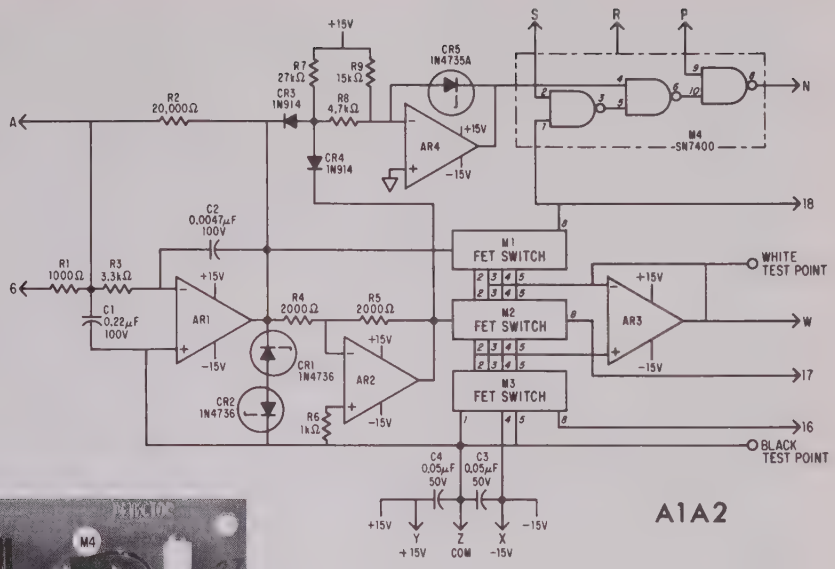


Figure 5-3. Detector Assembly (20890)

This assembly has the second (final) gain stage of the detector section (operational amplifier AR1), a unity-gain, inverting amplifier used in the auto-zeroing procedure (operational amplifier AR2), three FET analog switch modules used in the auto-zeroing procedure (M1 to M3), a unity-gain non-inverting amplifier buffering the output of the FET switch modules (operational amplifier AR3), an overload sensing detector (operational amplifier AR4), and a logic module (M4) used to gate the output of the overload detector.

Capacitors C3 and C4 are used to reduce high-frequency noise and coupling problems on the ±15-volt buses.

Resistors R1 and R2 determine the closed-loop gain (-20) of operational amplifier AR1. If the bridge has the same deviation errors on all combinations of bridge ranges and deviation ranges, and the generator voltages are correct, R1 and/or R2 may be faulty or there may be low open-loop gain in AR1.

Capacitors C1 and C2 and resistor R3 are used to attenuate high-frequency noise on the detector signal. Their values are rather non-critical. However, if resistor R3 opened, then the Model 280 would probably display near-zero deviations at all times, and if C1 or C2 had low internal resistance, it could cause the deviation indications to be low on all combinations of bridge ranges and deviation ranges.

Diodes CR1 and CR2 are used to limit the output of AR1 to about ±8 volts because the maximum voltage rating of FET switch modules is ±10 volts.

Resistors R4 and R5 determine the closed-loop gain (-1) of operational amplifier AR2. If the same deviation errors occur on all combinations of bridge ranges and deviation ranges, the generator voltages are correct and the instrument will not correctly eliminate the effect of thermal emf's in the bridge, R4 and/or R5 may be faulty or there may be low open-loop gain in AR2.

Resistor R6 is used to reduce the effects of bias current drift in AR2. The value of R6 is relatively non-critical.

AR2 is the first amplifier in the detector section of the bridge whose input voltage drifts will not be cancelled out in the auto-zeroing procedure. However, considering the temperature and time stability of the amplifiers that are used, it would take a large drift (one millivolt) in the input voltage offset of either AR2 or AR3 to cause one least significant digit drift in the display of the Model 280.

The FET analog switch modules M1, M2 and M3 connect the detector section amplifier output to the input of the analog-digital convertor assembly (ESI Part No. 20909). Switch M1 is closed (Pin 18, less than 1/2 volt) during the first integration of the detector signal. Switch M3 is closed (Pin 16, less than 1/2 volt) during the time between the two detector signal integrations (while the bridge output is settling after generator polarity reversal). Switch M2 is closed (Pin 17, less than 1/2 volt) during the second integration of the detector signal. M2 may operate before M1 in some Model 280's.

Operational amplifier AR3 is connected in a unity-gain non-inverting mode. Low gain in AR3 would cause deviation readings to be small on all combinations of bridge ranges and deviation ranges.

AR4, CR3, CR4, CR5, R7, R8 and R9 form a circuit that will detect when the detector section of the Model 280 is nearing saturation. Logic gate M4 gates the overload signal to light the overload indication if the detector is overloaded during the first period of detector signal integration.

If the Φ remains unlit when the Model 280 indicates near-zero deviation and the bridge is badly overloaded or when it produces wrong answers in the presence of large thermal emf's of hum pickup, the problem might be in the overload detection circuitry.

If the overload detection circuitry is working correctly, during the first detector signal integration, the voltage on Pin N will exceed 3 volts only when the voltage on the white test point exceeds ±5 or 6 volts. It is assumed that an overload during the first integration

will also exist during the second integration. (The timing of switches M1 and M2 may be reversed so that the "first integration" may actually be the second.) In addition, the overload detection point is set about 25% below the actual detector saturation point. The voltages on the white test point can be varied by deviating the bridge.

Typical waveforms observed with an oscilloscope on the white test point of the detector assembly are shown in Figure 5-4.

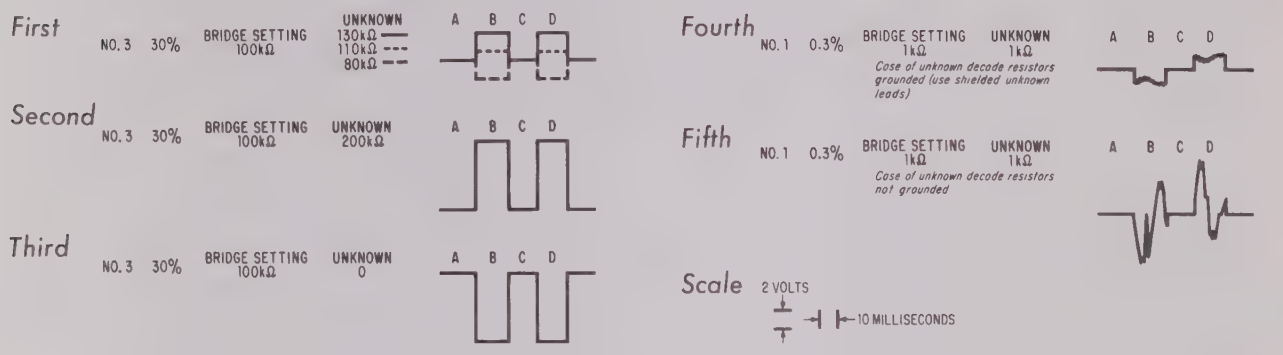

First
NO. 3 30% BRIDGE SETTING 100kΩ UNKNOWN 130kΩ 110kΩ 80kΩ
A B C D
Second
NO. 3 30% BRIDGE SETTING 100kΩ UNKNOWN 200kΩ
A B C D
Third
NO. 3 30% BRIDGE SETTING 100kΩ UNKNOWN 0
A B C D
Fourth
NO. 1 0.3% BRIDGE SETTING 1kΩ UNKNOWN 1kΩ
Case of unknown decade resistors grounded (use shielded unknown leads)
A B C D
Fifth
NO. 1 0.3% BRIDGE SETTING 1kΩ UNKNOWN 1kΩ
Case of unknown decade resistors not grounded
A B C D
Scale 2 VOLTS
10 MILLISECONDS

Figure 5-4. Typical Waveforms

The Model 280 was in the CONTINUOUS MODE. The external trigger for the oscilloscope was the negative-going voltage spike on the left end of the 0.1 microfarad capacitor located in the upper lefthand corner of the logic interface assembly (ESI Part No. 19908).

Section A of each waveform includes the 1/60-second first settling period, the 3-1/3-millisecond conversion complete signal, and the typically less-than-1-millisecond analog-to digital converter reset time.

Section B is the detector output signal for the first integration. It is always 1/60 second long.

Section C is the signal presented to the analog-to-digital converter while the bridge settles after generator polarity reversal. It is always 1/60 second. Section C must always be a zero-volt signal (less than 5 millivolts) or the deviation display could have zero offsets, non-linearity and other problems. A non-zero signal in section C could be caused by switches M1 and M2 being on (they should be turned off with high-state logic signals on Pins 17 and 18), switch M3 being off (it should be on with a low-state logic signal on Pin 16), or faulty diodes CR1 and CR2, resulting in inadequate limiting of the output of operational amplifier AR1.

Section D is the detector output signal for the second integration. It is always 1/60 second long.

The waveform repeats after section D.

The first waveform shows the detector output with the detector preamplifier at its lowest gain The low gain, shielded unknown leads and grounding of the case of the "unknown" decade resistor should result in almost no observable 60 Hz signal. The average value of the signals in sections B and D should result in 10% deviation per 1 volt (average) of signal. The voltage in section B should not differ from that in section D by more than 100 millivolts. If it does, pull out the detector preamplifier assembly and observe if the section B signal is still more than 100 mV different from that in section D. If it is then the problem is on the detector assembly, probably due to a fault in AR1, AR2, R4 or R5.

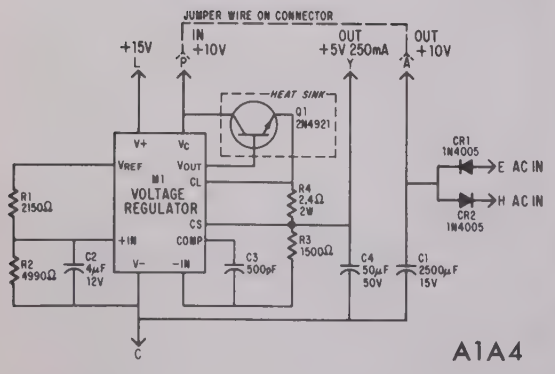
The second and third waveforms show the detector output when the bridge is overloaded in either direction. The fact that the signals in sections B and D are greater than 7 volts shows that the amplifiers on the detector assembly have sufficient output swing capability. The fact that the signals are limited at 8 volts shows that the limiting diodes CR1 and CR2 are probably not faulty.

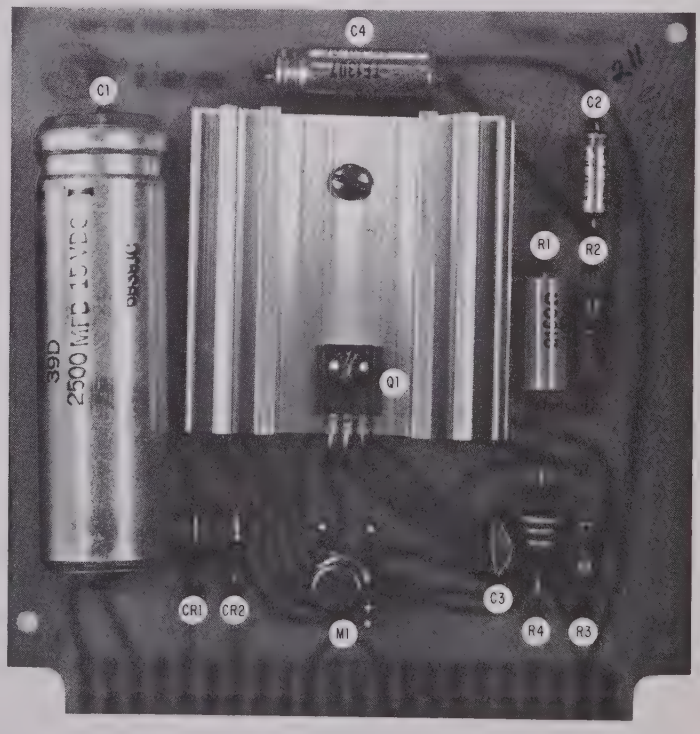
The fourth waveform shows the detector output when the detector preamplifier is at its highest gain. Even though shielded unknown leads are used, and the case of the decade resistor used as the unknown is grounded, some 60 Hz pickup is observed because the case of the Model 280 is open and there is some 60 Hz noise from the generator output. Also some higher frequency noise is observed that is probably due to the detector preamplifier. If a high-quality decade resistor is used as the unknown resistor (reasonably low thermal emf's) and the deviation indication is near zero, then the offset of sections B and D from zero is mostly due to voltage offset in the detector preamplifier. The average offset should be less than 1.5 volts.

The fifth waveform shows the detector output when the detector preamplifier is at its highest gain and with the case of the "unknown" decade resistor floating (not tied to ground). The ungrounded case causes the large amount of hum pickup; however, the actual amount will depend on the nearness of power cords, etc. The "overload switching spike" occurs when the overload detection circuit, using operational amplifier AR4, changes state. This may not be observable on some Model 280's. If the setting of the bridge and "unknown" resistor are reduced together in 100-ohm increments, the 60 Hz pickup will gradually reduce and the hum level can be found where the Φ indication just comes on (the deviation indication should be near zero). This should occur approximately when the maximum excursion of the hum voltage peaks is 5 volts relative to the voltage in section C of the waveform.

5.1.4 5-Volt, 250-Milliamp Supply Assembly

ESI Part No. 19883





A1A4

Figure 5-5. 5 V, 250 mA Supply Assembly (19883)

This assembly (see Figure 5-5) has a single 5-volt regulator. The output of this supply is used in the Model 280 as the power source for the logic in the detector section.

The source of the unregulated ac voltage, the center-tapped transformer winding, connects to the circuit on Pins E, C, and H. Pin C is the common bus of the circuit and is also the low side (-) of the output. The +5-volt output is on Pin Y.

Diodes CR1 and CR2 rectify the unregulated ac voltage.

Capacitor C1 filters the rectified ac voltage. The unregulated dc voltage on capacitor C1 is the source of current for the output of the supply and is connected to Pins A and P. The value of the unregulated dc voltage, depending on line voltage, is approximately 10 volts.

The integrated circuit voltage regulator M1 has a voltage reference, an error amplifier, a series pass transistor, and provision for current limiting. An additional series pass transistor Q1 is used in the 5-volt supply because the transistor internal to the integrated circuit does not have sufficient current or power capability. The voltage regulator is powered by a 15-volt supply external to the board that connects to the circuit on Pin L.

Capacitor C2 filters the internal voltage reference of M1 and reduces the noise in the output. If C2 has low internal resistance, the output of the 5-volt regulator will be low.

Resistors R1 and R2 set the output voltage. If the value of R2 is raised, the output of the circuit will be higher. If the value of R1 is raised, the output of the circuit will be lower.

Resistor R3 reduces drifts in the output of the 5-volt regulator caused by changing bias currents in M1. Errors in its value will probably have small effect on the value of the output voltage.

Resistor R4 sets the current-limiting level of the output. When the voltage drop across R4 increases to approximately 0.65 volts, the output current will limit.

Capacitor C3 stabilizes the error amplifier in M1. If C3 were faulty, it could cause errors in the output voltage or circuit oscillations.

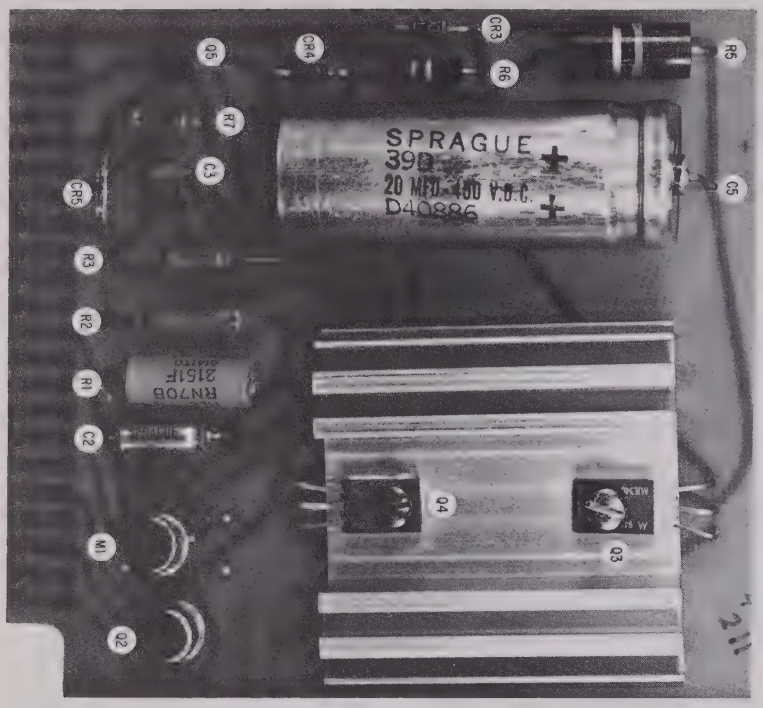
Capacitor C4 is the final output filter. An open capacitor could result in excessive output noise or ripple. A capacitor with low internal resistance could result in reduced current available to the load. The voltage on C4 should be between 4.7 and 5.3 volts, and should have less than 100 millivolts peak-to-peak ripple.

5.1.5 200-Volt and 5-Volt Supplies Assembly

ESI Part No. 19879

This assembly has a 200-volt regulator and part of a 5-volt regulator. The 200-volt regulator is used to light the display tubes and panel lights on the Model 280. The 5-volt regulator is the power source for the logic in the logic section. The parts of the 5-volt regulator that are not mounted on the assembly are located on the heat sink that is bolted to the side of the chassis, directly behind the display tubes.

The circuit of the 5-volt regulator (ignoring component values), is almost the same as the 5-volt regulator on the 5 V, 250 mA supply assembly (ESI Part No. 19883) except that capacitor C4 is eliminated and transistor Q1 is replaced by two transistors, Q1 and Q2. Capacitor C4 is eliminated because final filtering and high-frequency by-passing of the 5-volt supply



WARNING

Use caution when working on or around this circuit. The 200-volt supply can shock you.

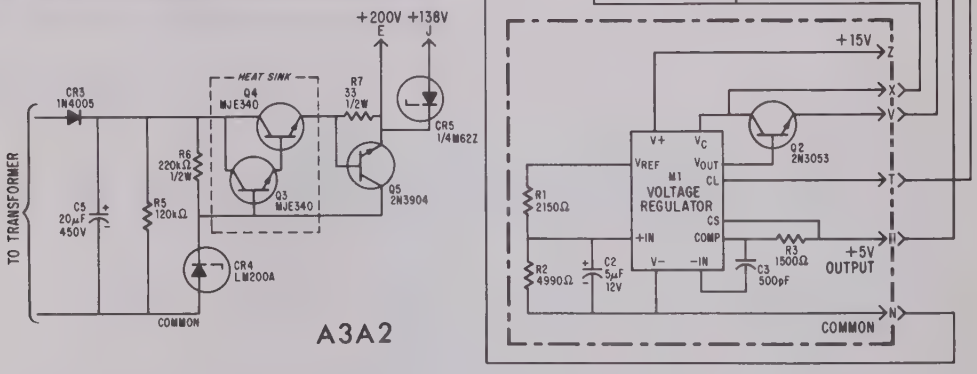


Figure 5-6. 200-Volt and 5-Volt Logic Supplies Assembly (19879)

is accomplished where the current is used. Q1 and Q2 are connected as a Darlington pair to increase current gain and perform the same function as the one transistor on the 5 V, 250 mA supply assembly. To help in understanding the operation of this circuit, respective components of both circuits are numbered the same.

The source of the unregulated ac voltage used for the 200-volt supply, the transformer winding, connects to the circuit on Pins A and C.

Diode CR3 half-wave recitifies the unregulated ac voltage.

Capacitor C5 filters the rectified ac voltage. The value of the unregulated dc voltage on C5 depending on line voltage, approximately 240 volts.

Resistor R5 is a bleed resistor to discharge C5 when the instrument is turned off so that a hazardous voltage will not remain on C5.

Resistor R6 supplies the current for the voltage reference diode CR4.

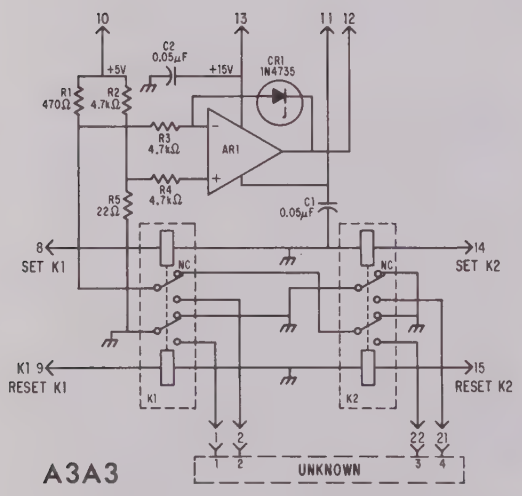
Transistor Q4 is the series pass transistor for the 200-volt supply. Transistor Q3 is connected to it in a Darlington configuration for increased current gain. The extra current gain is needed in order to prevent beta variations in Q4 or load variations on the supply from causing excessive current in CR4. If the output of the 200-volt supply is too high, it is probably caused by emitter-to-collector shorts in the transistors or failure of CR4.

Resistor R7 is a current shunt. When the voltage drop across R7 increases to about 0.7 volts, excessive loading of the supply, it will cause transistor Q5 to turn on. The voltage across CR4 will reduce and the current from the supply will limit.

Zener diode CR5 is used to drop the voltage of the 200-volt supply for use on small neon bulbs. If the display tubes are working properly, but the RESET, LEAD FAIL, and MEASURE lights are inoperative, it could be caused by failure of this diode.

5.1.6 Lead Check Circuit Assembly

ESI Part No. 19890



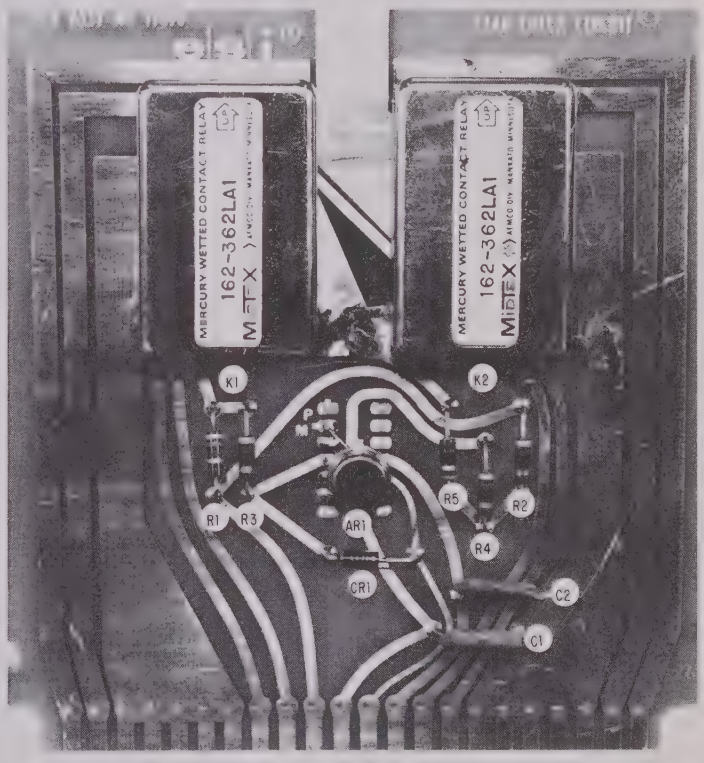


Figure 5-7. Lead Check Circuit Assembly (19890)

This assembly (see Figure 5-7) contains the circuitry and relays used to verify the connection of a Model 280 to the unknown resistor by measuring the resistance of the unknown leads. In a Kelvin resistance bridge deviation readings that appear to indicate a good resistor may occur when the bridge is inoperative. For instance, if the lead from the generator to the unknown is open, there will be no voltage applied to the bridge and all values of unknown resistors will register zero deviation. If the yoke lead is open when low-value resistors are being measured, the yoke arms are being compared to the main arms, with some small fraction of the deviation caused by errors in the unknown, so that the deviation could seem quite

reasonable even when the unknown resistor had gross errors. These problems are eliminated in the Model 280 by checking the lead resistance before each measurement or sequence of measurements. If the unknown is not in the test fixture and the test fixture contacts do not touch, a lead failure will be indicated by the LEAD FAIL lamp. If the contacts do touch the display will always indicate an overload.

A lead check is initiated each time a start command is given to the Model 280. In the CONTINUOUS MODE of operation, a lead check is performed only before the first measurement in the series.

The magnetic, latching mercury-wetted relays K1 and K2 are shown in the reset position. When K1 only is in the set position, the leads connected to UNKNOWN terminals 1 and 2 are checked by connecting them to the lead measurement bridge. When K2 only is in the set position, the leads connected to UNKNOWN terminals 3 and 4 are checked. When both relays are in the set position, when the Model 280 is in its reset state, UNKNOWN terminals 1 and 4 are connected together by connecting both to ground, so that the feedback loop of the generator will be completed and the generator will not saturate or cause the current limit relay to chatter from hum pickup.

Note that when both relays are in the reset position, as during a bridge measurement, the only parts of the relays that are not grounded are connected to the UNKNOWN terminals. This prevents voltage on the lead check bridge from causing errors in the measurement bridge. In addition, there is no voltage on the relay coils during a measurement because the relays are latching types and are driven by 3-millisecond pulses. Also note that the board has field-effect type guarding, has grounded groups of connector pins between both pairs of leads connecting to the UNKNOWN terminals and the active circuitry, and has maximum separation of the leads that connect to either end of the unknown resistor. This prevents the assembly insulation from shunting the unknown resistor.

The lead check circuit insulation can shunt the 10-kilohm bridge arm. The effect of this shunting can be tested by unplugging the lead check circuit assembly. A deviation reading should not change by more than 0.0001% when this is done unless the instrument is exposed to excessive humidity or the lead check circuit is dirty. Be careful with the lead check assembly; handle it by the edges and do not get it greasy or dirty.

Unplug the lead check circuit when the Model 280 must be operated in a position other than its normal one (bottom within 30 degrees of horizontal) for troubleshooting purposes.

Resistors R1, R2 and R5 make up the bridge that measures the lead resistances. The bridge will balance when the sum of the two leads being tested is 2 ohms (±1/2 ohm). If all the resistance were due to a poor connection in the number 2 unknown lead, the resulting bridge error would be 0.02%. If the sum of the two leads being tested is greater than 2 ohms, the output from the lead test bridge to amplifier AR1 will reverse polarity, the output of AR1 will change state, and a lead failure will be indicated on the front panel.

The lead check test level can be adjusted by varying the value of resistor R5. The lead check test level is approximately 1/10 of the value of R5. Any value of R5 is aaceptable if it is less than 10 kilohms and the resulting lead check test level is sufficiently accurate and stable to satisfy the operator.

Zener diode CR1 causes the output of AR1 to limit at approximately zero and +5 volts. Since AR1 has high gain, even small unbalances of the lead check bridge (less than 0.1 ohm unbalance) will cause the output of AR1 to be either 0 volts or +5 volts. The output of AR1 connects directly to the logic of the Model 280.

Resistor R3 limits the current that AR1 must deliver.

Resistor R4 reduces drifts in the lead check test level caused by drifts in the bias current of AR1. Its value is relatively non-critical.

Capacitors C1 and C2 are power supply bypass capacitors.

5.1.7 Generator and Bridge

The generator of the ESI Model 280 supplies the voltage for the bridge circuit in a manner that holds the voltage across the standard constant on any given combination of bridge and deviation ranges. This results in constant current in the unknown on any given combination of ranges and linear deviation voltages to the detector for any deviation. Figure 5-8 is a simplified schematic of the generator and bridge.

The generator of the Model 280 will hold constant voltage on the standard until its output voltage capability is exceeded (approximately 35 volts at 90 volts ac line) or its current limit is reached. The deviation display will indicate an overload before the voltage limit is reached. The current limit is set so that the bridge cannot be harmed by the generator.

The generator voltages and current limits are shown in Table 5-2. The upper numbers are voltages on the standard. The middle numbers are voltages on the unknown at zero deviation (the voltage on the unknown is proportional to its value). The lower numbers are current limits.

	DEVIATION RANGE	BRIDGE RANGE 1	2	3	4	5
Voltage On Standard	0.3%	25 V	25 V	7.9057 V	2.5 V	0.25 V
	3.0%	7.9057 V	7.9057 V	2.5 V	0.79057 V	0.25 V
	30%	2.5 V	2.5 V	0.79057 V	0.25 V	0.25 V
Voltage On Unknown At 0 Deviation	0.3%	0.25 V	2.5 V	7.9057 V	25 V	25 V
	3.0%	79.05 mV	0.79057 V	2.5 V	7.9057 V	25 V
	30%	25 mV	0.25 V	0.79057 V	2.5 V	25 V
Current Limit	0.3%	27.77 mA	27.77 mA	87.84 mA	27.77 mA	27.77 mA
	3.0%	87.84 mA	87.84 mA	27.77 mA	87.84 mA	27.77 mA
	30%	277.7 mA	277.7 mA	87.84 mA	27.77 mA	27.77 mA

Table 5-2. Generator Voltages and Current Limits

Note that the generator voltages always change by a factor of 10 or the square root of 10 when ranges are changed. This simplifies power calculations when the same resistor is measured on different ranges.

The voltages in Table 5-2 are the voltage changes that occur when the generator is turned on in either polarity. Because the Model 280 is auto-zeroing it is the voltage *changes* in the bridge that cause the indicated deviations. The level at which they change is relatively unimportant. For instance, when a resistor is measured on BRIDGE RANGE Ω_1 using DEVIATION RANGE 0.3%, the voltage across the standard is 25 volts in each polarity and the voltage change from one polarity to the other is 50 volts. If the generator had a large voltage offset, 5 volts for instance, the voltage across the standard would change from +30 volts to

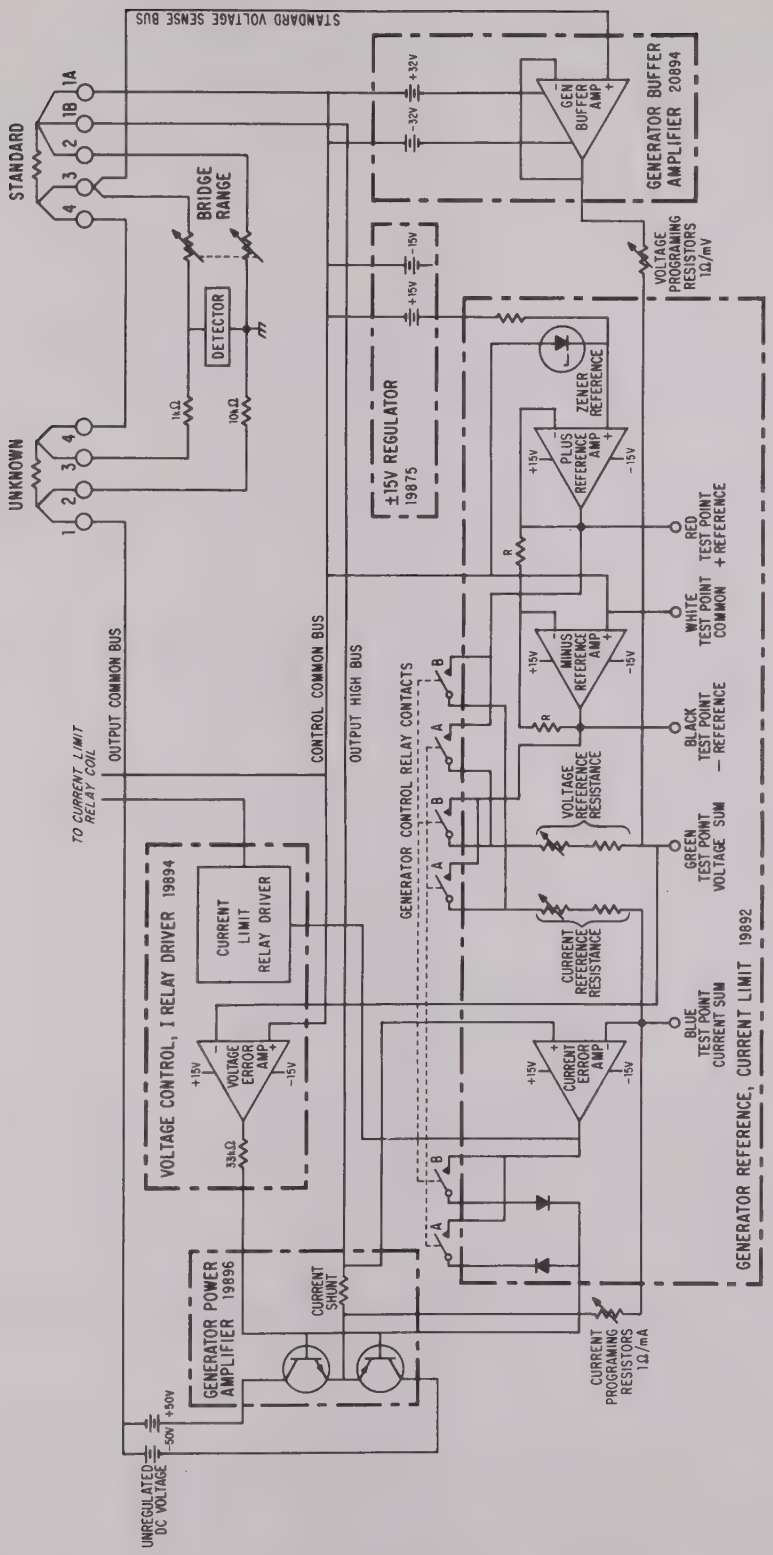


Figure 5-8. Generator and Bridge Simplified Schematic

-20 volts, but the change would still be 50 volts and the Model 280 would still give the same deviation reading. The typical voltage offset of the Model 280 generator is actually less than a few millivolts.

The accuracy of the generator voltages should be 0.1%. However, if all the generator voltages are in error by a larger amount but by the same percentage, it might be possible to trim the analog-to-digital converter in the detector section (ESI Part No. 20909) so that the deviations are still correct. The accuracy of the generator current limits should be ±10%.

The inputs and outputs of the generator section are as follows:

1. Power via transformer primary
2. Plus on signal via coil of guarded reed relay (contacts labeled "A" in Figure 5-8)
3. Minus on signal via coil of guarded reed relay (contacts labeled "B" in Figure 5-8)
4. Current-limit signal via contacts of current-limit relay (contacts of this guarded reed relay will be open when the output of generator is current limited)
5. Voltage and current programing information via position of rotary switches mounted on generator box
6. Generator current output leads connected to STANDARD terminal 1B and UNKNOWN terminal 1
7. Generator voltage sensing leads connected to STANDARD terminals 1A and 3

The low side of the generator output, the output common bus, connects to UNKNOWN terminal 1 and the generator guard box. The guard box concentrates virtually all of the leakage resistance of the generator to ground on the bridge corner that is most tolerant of leakage resistance.

The high side of the generator output, the output high bus, connects to STANDARD terminal 1B.

The generator voltage sensing lead on the generator end of the standard, the control common bus, connects to STANDARD terminal 1A.

The generator voltage sensing lead on the yoke end of the standard, the standard voltage sense bus, connects to STANDARD terminal 3. This lead connects to the input of the generator buffer amplifier (ESI Part No. 20894, see Figure 5-12). The generator buffer amplifier is a unity gain non-inverting amplifier using a higher voltage FET operational amplifier to provide a very high input impedence (greater than 100,000 megohms) so that no significant current will flow along the standard voltage sense bus and affect the accuracy of the bridge.

Because the generator buffer amplifier must handle 25-volt input signals, it has its own power supplies on its assembly (±32 volts). The rest of generator control circuitry is powered by the ±15-volt regulator (ESI Part No. 19875, see Figure 5-1).

The voltage reference for the generator is a Zener reference diode that is powered by the ±15-volt supply. The Zener is buffered by a unity gain non-inverting amplifier, the plus reference amplifier, whose output is referred to as the "plus reference". The "minus reference" is the output of a unity gain inverting amplifier, the minus reference amplifier. The plus and minus references should be within 0.1% of the same absolute value.

In the following discussion, all test point voltages are relative to the white test point that is connected to the control common bus. Since the generator is not grounded in the Model 280 and the generator control common bus will differ from the potential of the generator guard box by the output of generator, a battery-powered or passive voltmeter or a differential input oscilloscope should be used to observe the voltages on the test points. The deviation readings of the Model 280 will probably be affected (especially when an oscilloscope is used).

The plus reference can be checked by reading the voltage on the red test point. The minus reference can be checked by reading the voltage on the black test point. Each voltage should be between 5.9 and 6.5 volts.

When the generator is voltage regulating, the voltage at the green test point will be near zero (typically less than 1 millivolt). When the generator is current limited, the voltage at the blue test point will be near zero (typically less than 3 millivolts). In other words, the input of the appropriate error amplifier (voltage error amplifier or current error amplifier) will be near zero when the generator has its output under control.

When the generator is off, neither generator relay will be energized and contacts labeled A and B will all be open. When the generator is on with the output positive (STANDARD terminals 1A and 1B positive with respect to UNKNOWN terminal 1), the A contacts will be closed.

When the generator is off, its output voltage will be primarily determined by the voltage offsets of the generator buffer amplifier and the voltage error amplifier, and will be typically less than 2 millivolts.

When the generator is on, and its output is voltage regulated, the ratio of the reference voltage to the output voltage is equal to the ratio of the voltage reference resistance to the voltage programing resistance, and the green-test-point voltage is near zero (typically less than 1 millivolt).

When the generator is on, and its output is current limited, the ratio of the reference voltage to the voltage drop across the current shunt is equal to the ratio of the current reference resistance to the current programing resistance, and the blue-test-point voltage is near zero (typically less than 3 millivolts).

When the generator is on, and its output is voltage regulated with the output current below the current limiting level, the output of the current error amplifier will swing in the direction that would increase the current output (thereby taking the generator out of voltage regulation). but the current output will not increase because the diode switched in series with the output of the current error amplifier will only let the output of the amplifier decrease (i.e. limit) the current output of the generator.

When the generator is on, and its output is current limited, one of the diodes in series with the output of current error amplifier will be conducting (whichever one is switched into the circuit) and the output of the current error amplifier will be opposing the output of the voltage error amplifier. When the generator is current limited the voltage error amplifier will be trying to increase the output of the generator. The current error amplifier will be able to limit the output because the conducting diode on the output of the current error amplifier will be lower resistance than the 33-kilohm resistor on the output of the voltage error amplifier, and the current error amplifier will take over control of the generator power amplifier.

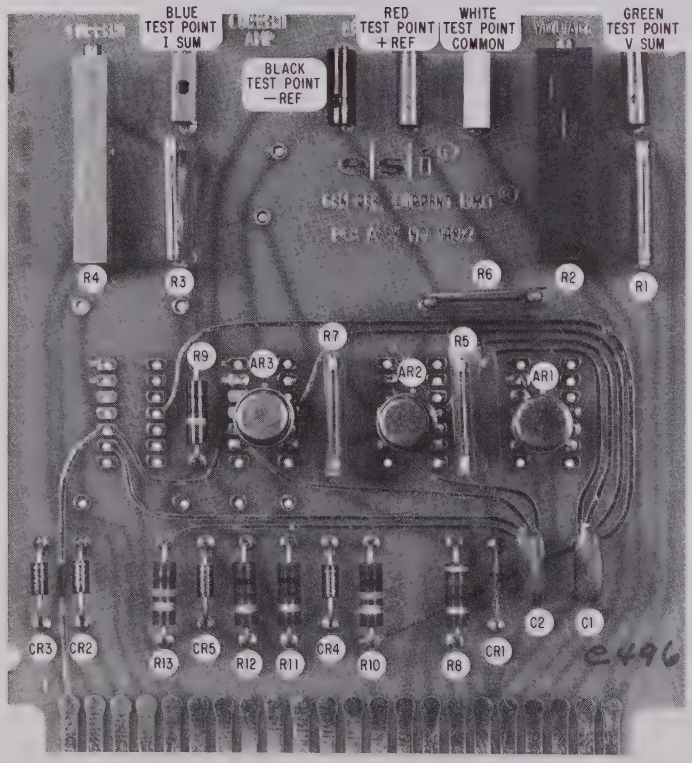
The generator power amplifier is a class B amplifier, and it takes a very small voltage swing on its input to turn it hard on in either polarity. As a result, the output of the current error

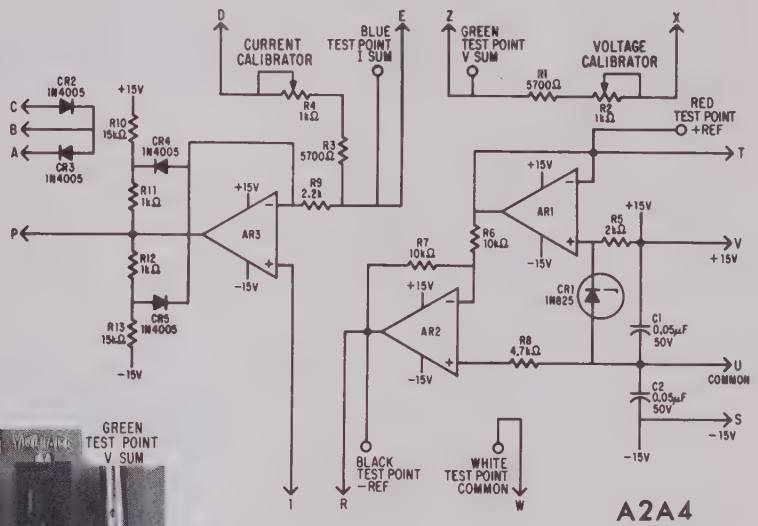
amplifier will only be about one diode's voltage drop (about 0.7 volts) away from the control common bus when the generator output is current limited. On the other hand, when the generator output is voltage regulated, the diode on the output of the current error amplifier (whichever one is switched into the circuit) will not conduct, and the output of that amplifier will swing away from the control common bus until it voltage limits. In other words, the output of the current error amplifier will be larger when the generator is voltage regulated than when it is current limited.

The current limit relay driver senses the output voltage swing of the current error amplifier and causes the current limit relay to open when the generator is current limited.

5.1.8 Generator Reference and Current Limit Assembly

ESI Part No. 19892





NOTE

All test point voltages on this assembly are measured relative to the white test point and should be measured with a floatation voltmeter or a differential input oscilloscope. When the test point voltages are measured, the deviation readings of the Model 280 will probably be affected.

Figure 5-9. Generator Reference and Current Limit Assembly (19892)

This assembly (see Figure 5-9) contains part of the Model 280 generator circuit. The principal parts on this assembly are the voltage reference CR1, the current error amplifier AR3, the voltage reference resistors R1 and R2, and the current reference resistors R3 and R4.

Zener reference diode CR1 is the voltage reference for both the plus reference (red test point) and the minus reference (black test point). Its voltage should be between 5.9 and 6.5 volts.

Resistor R5 supplies the current for CR1. If both the plus reference and minus reference measure zero, R5 might be open.

Operational amplifier AR1 is wired as a unity-gain non-inverting amplifier and buffers the zener reference diode CR1. Its output is the plus reference.

Operational amplifier AR2 and resistor R6 and R7 form a unity-gain inverting amplifier whose output is the minus reference. Resistor R8 reduces errors caused by the offset current AR2. If the plus reference does not match the minus reference (within 0.1%), it is probably due to a problem in one of these four components.

Resistors R1 and R2 make up the voltage reference resistance. R2 is adjusted to calibrate the voltage output of the generator. If all of the generator voltage outputs (voltage change from plus to minus polarity) are in error by the same percentage, R2 needs adjustment. If only some of the generator voltages are in error, the generator programing resistors or the switching for those resistors may be the cause.

Resistors R3 and R4 make up the current reference resistance. R4 is adjusted to calibrate the current limiting of the generator. If all of the generator current limits are in error by the same percentage, R4 needs adjustment. If only some of the current limits are in error, the current programing resistors or the switching for those resistors may be the cause.

Operational amplifier AR3 is the current error amplifier. When the generator is current limited its input (blue test point) will have zero voltage relative to the control common bus (white test point).

Capacitor C3 and Resistor R9 are frequency compensation components that help to stabilize the control loop when the generator is current limited.

Resistors R10, R11, R12, and R13 and diodes CR4 and CR5 limit the voltage swing of AR3 and keep it from saturating so that AR3 can more quickly limit the generator current when the need arises. If the output of AR3 swings to -1.7 volts (±0.2 volts), diode CR4 will conduct, causing the output of AR3 to limit. The same thing will happen in a plus direction except that diode CR5 will conduct. If the current overload relay coil is not energized (causing an overload indication on the Model 280), one of these components could be the cause.

Diodes CR2 and CR3 are switched in series with the output of AR3 and the input of generator power amplifier. CR2 is used when the output of the generator is positive (STANDARD terminal 1A positive with respect to UNKNOWN terminal 1). CR3 is used when the output of the generator is negative. The diode polarity is such that the current error amplifier AR3 can reduce the output current, but cannot increase it.

The generator control relays (guarded reed relays that turn the generator on) make connections between edge connector pins on the generator reference, current limit assembly as follows:

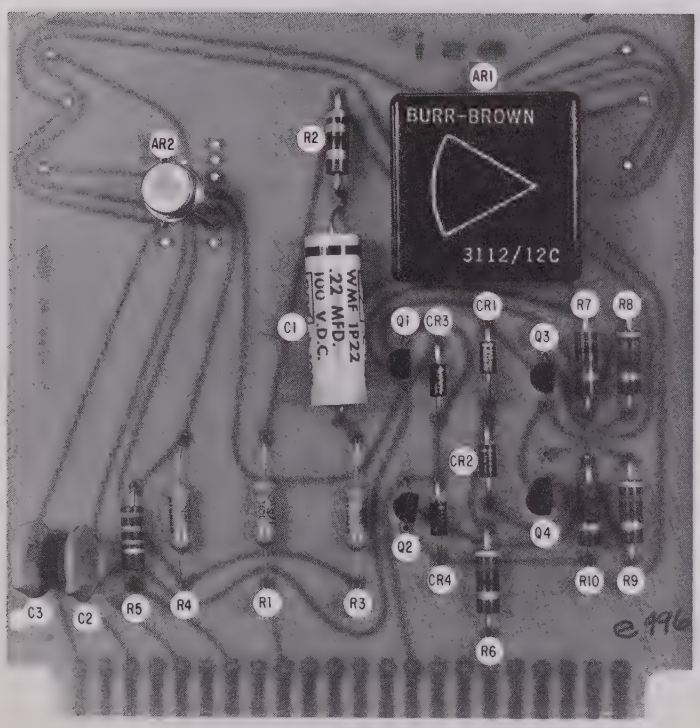
Generator Output Positive	Generator Output Negative
X to T	X to R
D to R	D to T
P to C	P to A

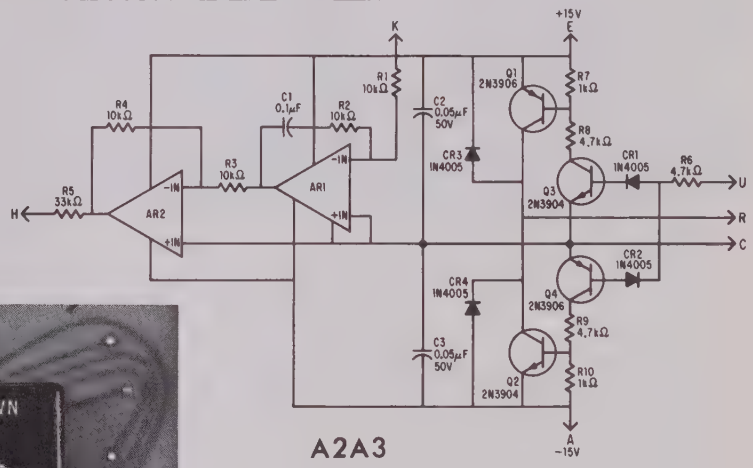
Capacitors C1 and C2 are high frequency bypass capacitors used to reduce noise and coupling on the power supply lines.

The white test point ties to the control common bus at a central tie point, Pin C on the voltage control and current limit relay driver assembly (ESI Part No. 19894, see Figure 5-10).

5.1.9 Voltage Control and Current Limit Relay Driver Assembly

ESI Part No. 19894





NOTE *REFERENCE DESIGNATIONS OF COMPONENTS IN ASSEMBLIES AND SUBASSEMBLIES ARE ABBREVIATED FOR CLARITY. PREFIX DESIGNATION WITH DESIGNATION OF ASSEMBLY WHEN REFERING TO COMPONENT OUT OF CONTEXT. FOR EXAMPLE, C1 IN ASSEMBLY A1 SHOULD BE A1C1, R2 IN ASSEMBLY A2 SHOULD BE A2R2, SUBASSEMBLY A1 IN ASSEMBLY A2 SHOULD BE A2A1, AND R3 IN THAT SUBASSEMBLY SHOULD BE A2A1R3*

Figure 5-10. Voltage Control and Current Limit Relay Driver Assembly (19894)

This assembly contains part of the Model 280 generator circuit. The principal parts on this assembly are the voltage error amplifier AR1 and AR2 and the current limit relay driver.

The voltage error amplifier is actually made up of two operational amplifiers, AR1 and AR2. AR2, in conjunction with resistors R3 and R4, is a unity-gain inverting amplifier that is used because AR1 performs more satisfactorily as an inverting amplifier. R3 and R4 do not have to be particularly well matched. AR1 is the input amplifier of the voltage error amplifier and has a FET input.

Resistors R1 and R2 and capacitor C1 are frequency compensation components that help to stabilize the control loop when the generator is voltage limited. If the generator output oscillates, one of the components may be faulty (especially the capacitor).

Resistor R5 connects to the input of the generator power amplifier and allows the current error amplifier to take over control when the output of the generator should be current limited.

Capacitors C2 and C3 are high-frequency bypass capacitors used to reduce noise and coupling on the power supply lines.

All other components on the circuit board are part of the current limit relay driver. Pin U connects to the output of the current error amplifier. When the output of the current error amplifier exceeds 1.4 volts in either direction (i.e., when the output of the generator is voltage regulated), this circuit will energize the current limit relay coil by driving one end of the coil to either plus or minus 15 volts. If the generator output is positive (STANDARD terminal 1A positive with respect to UNKNOWN terminal 1), transistors Q1 and Q3 will be turned on and the relay coil will be driven to + 15 volts. If the generator output is negative, Q2 and Q4 will be turned on.

Resistor R6 limits the current the circuit will draw from the current error amplifier.

Diodes CR1 and CR2 raise the voltage level necessary to turn the current relay driver on, so that the generator will definitely be voltage regulating before the current limit relay is energized.

Resistors R8 and R9 limit the current drawn by the bases of Q1 and Q2, respectively.

Resistors R7 and R10 ensure that the leakage current in Q3 or Q4 will not turn on Q1 or Q2.

Diodes CR3 and CR4 are used to keep inductive kicks from the current limit relay from harming Q1 or Q2.

5.1.10 Generator Power Amplifier Assembly

ESI Part No. 19896

This assembly contains part of the Model 280 generator circuit. The principal parts on this assembly are the rectifiers CR1 through CR4, the current shunt R1, the power output transistors Q1 and Q2, and the driver transistors Q3 and Q4.

Diodes CR1, DR2, CR3 and CR4 rectify the unregulated ac voltage that becomes the generator output. The filter capacitors that these rectifiers supply are mounted on the generator guard box.

Resistor R1 is the current shunt for the generator. The voltage drop across this resistor is what causes the generator to current limit.

Transistors Q1 and Q2 are the power output transistors.

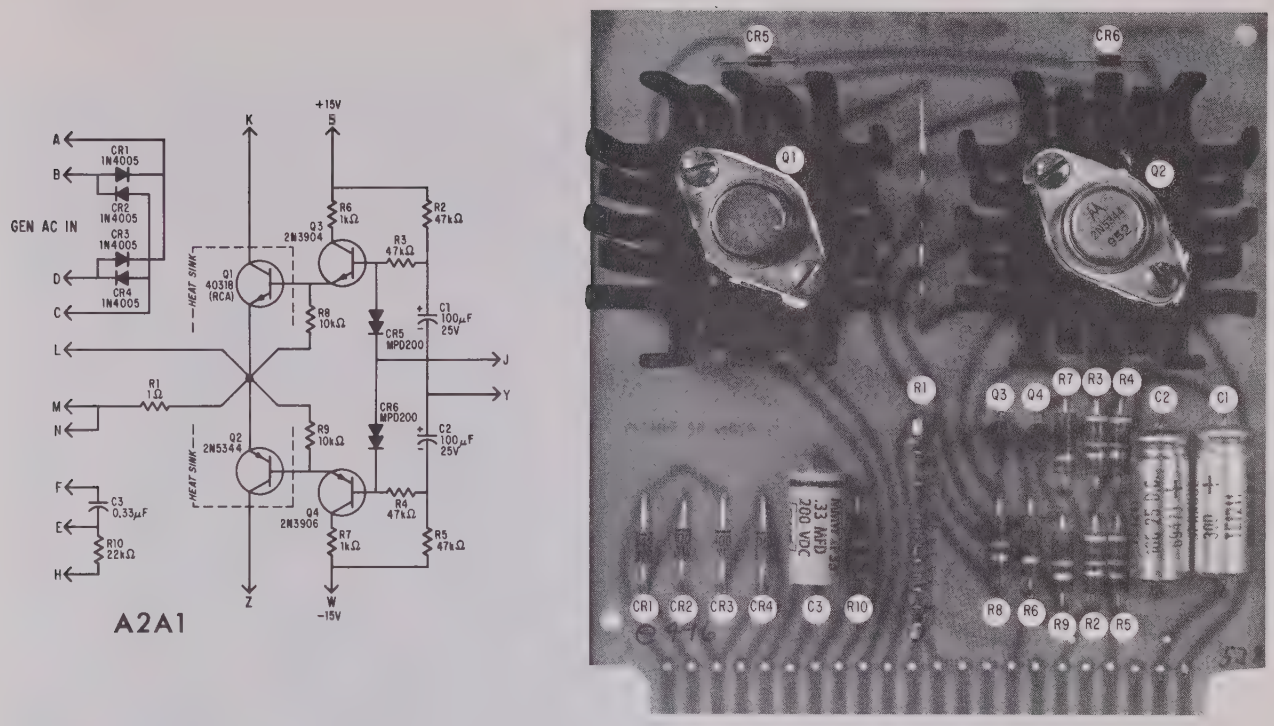


Figure 5-11. Generator Power Amplifier Assembly (19896)

Transistors Q3 and Q4 are the driver transistors for Q1 and Q2 respectively.

Resistors R6 and R7 limit the drive current in the bases of the power transistors.

Resistors R8 and R9 are to keep leakage currents from the drive transistors from turning on the power transistors.

Double diodes CR5 and CR6 bias the bases of the drive transistors to minimize the voltage swing at power amplifier input (Pin J) needed to swing the generator output from one polarity to the other. The power amplifier should be operating in class B mode and both power transistors should never be on at the same time. The quiescent current in the power output transistors should be less than 1 milliamp and can be verified by measuring the voltage drop across either of the 100-ohm power resistors that are mounted on the generator guard box near this assembly. The power resistors are in series with the collectors of the power transistors and the voltage drop across them when the generator is off (Model 280 in RESET), should be less than 0.1 volts.

Resistors R2, R3, R4 and R5 control the biasing current for CR5 and CR6.

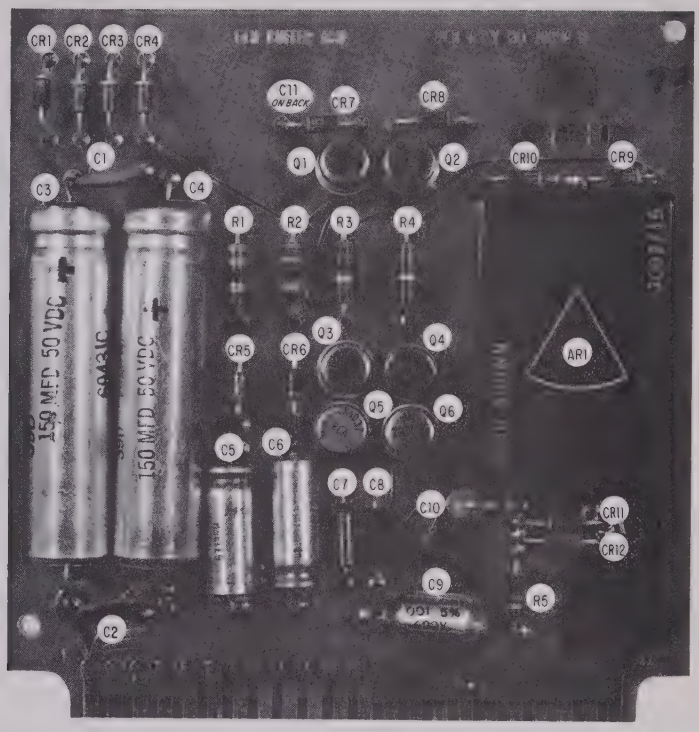
Capacitors C1 and C2 filter the biasing current for CR5 and CR6. The gain of the power amplifier is high enough that the output would have excessive hum without this filtering.

Capacitor C3 is connected across the output of the generator and is one of the components used to prevent oscillations.

Resistor R10 is connected so as to cause the output of the generator to return to zero faster when the generator is turned off.

5.1.11 Generator Buffer Amplifier Assembly

ESI Part No. 20894



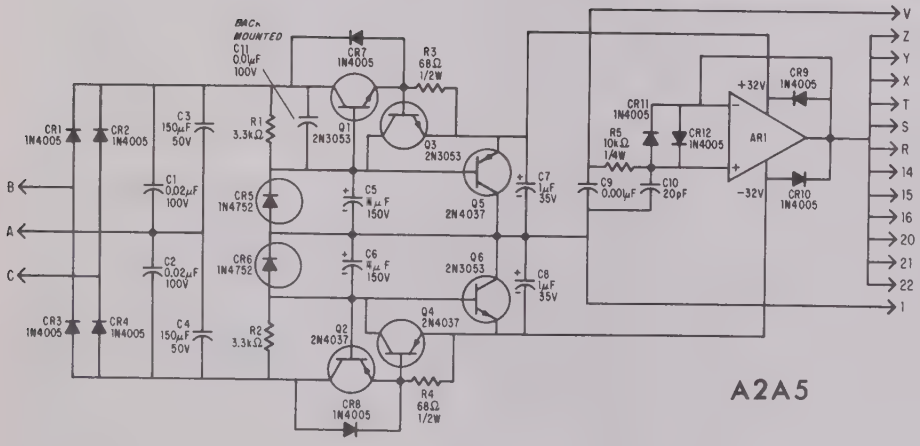


Figure 5-12. Generator Buffer Amplifier Assembly (20894)

This assembly (see Figure 5-12) contains part of the Model 280 generator circuit. The principal parts on this assembly are the buffer amplifier that is used to sample the voltage across the standard resistor and the power supplies for that amplifier. The buffer amplifier has its own power supplies because it needs different voltages than the other circuitry in the generator (±32 volts) and its power supplies need special overvoltage protection to protect the amplifier from excessive voltage inputs.

Operational amplifier AR1 is a high-gain FET input amplifier that is connected for non-inverting unity gain. Its operation can be checked by observing (with a differential input oscilloscope) that the voltage at Pin Z is within 1 millivolt of the voltage on Pin V except for short transients (1 and 2 millisecond) when the generator is turned on or off or reverses polarity.

Resistor R5 limits the current that will be driven into the input of AR1 when the generator output saturates or current limits.

Capacitors C9 and C10 are frequency compensation components that help to prevent oscillations in the generator.

Diodes CR11 and CR12 help to protect AR1 by limiting the maximum voltage difference between its inputs.

Diodes CR9 and CR10 help to protect AR1 by preventing its output from being driven more than the voltage drop of one diode past the power supply voltages.

The rest of the components on the assembly are part of the power supplies.

Diodes CR1, CR2, CR3 and CR4 rectify the unregulated ac voltage.

Capacitors C1, C2, C3 and C4 filter the unregulated dc voltage. The voltage across these capacitors should be approximately 40 volts (depending on the line voltage). Capacitors C1 and C2 are used to improve high frequency filtering (they have better high frequency characteristics than C3 and C4).

Resistors R1 and R2 supply the current for Zener diodes CR5 and CR6, respectively.

Capacitors C5 and C6 filter the voltage on the Zener diodes. The voltage across these capacitors should be between 31 and 35 volts.

Transistors Q1 and Q2 are the series pass transistors for the power supplies.

Diodes CR7 and CR8 protect the series pass transistors when the input of AR1 is severely overloaded and the output of AR1, because of the protection diodes around it, tries to swing past the power supply voltages. These components are redundant because the output of the power supplies is clamped by transistors Q5 and Q6. The diodes CR7 and CR8 should only be needed if Q5 and Q6 fail.

Transistors Q3 and Q4 cause the output of the power supplies to current limit when the voltage drop across R3 or R4 exceeds approximately 0.7 volts.

Capacitors C7 and C8 are the final output filters for the power supplies. The voltage across these capacitors should be between 30 and 34 volts.

5.2 BRIDGE LOGIC

5.2.1 Detector Logic

The basic function of the detector in the Model 280 is to determine the difference between two input-voltage levels presented to it at separate times; one when the generator is turned on in the positive direction and a different one when the generator is reversed.

The detector logic block diagram is shown in Figure 5-13. The detector logic consists of three major blocks of hardware, with four pulse transformers that connect the detector logic to the main logic. The three hardware blocks are circuit assemblies: the detector logic assembly, block 1; the detector assembly, block 2; and the integrator assembly, block 3.

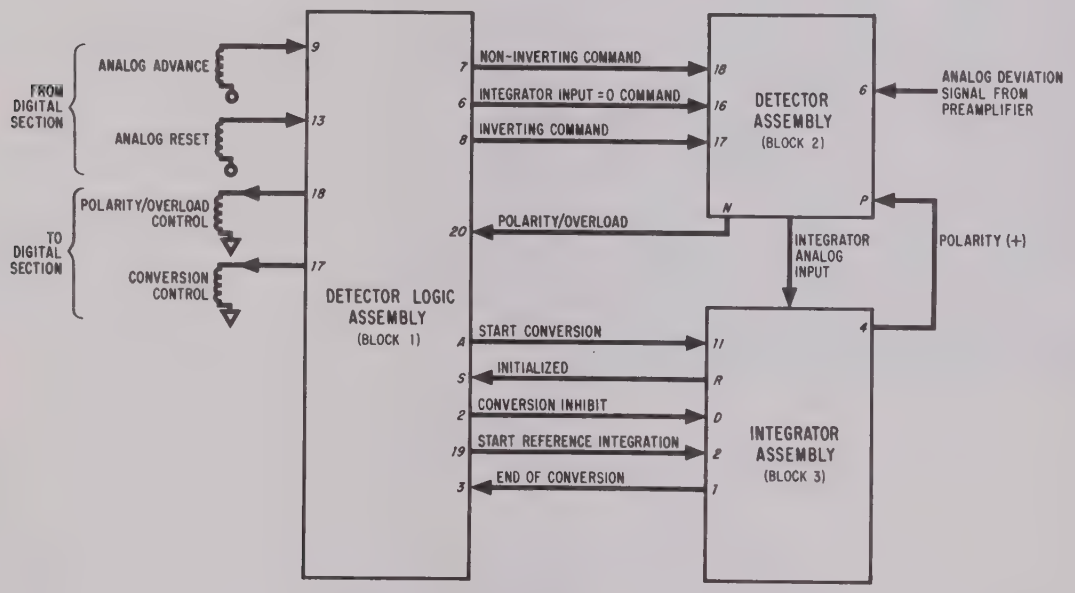
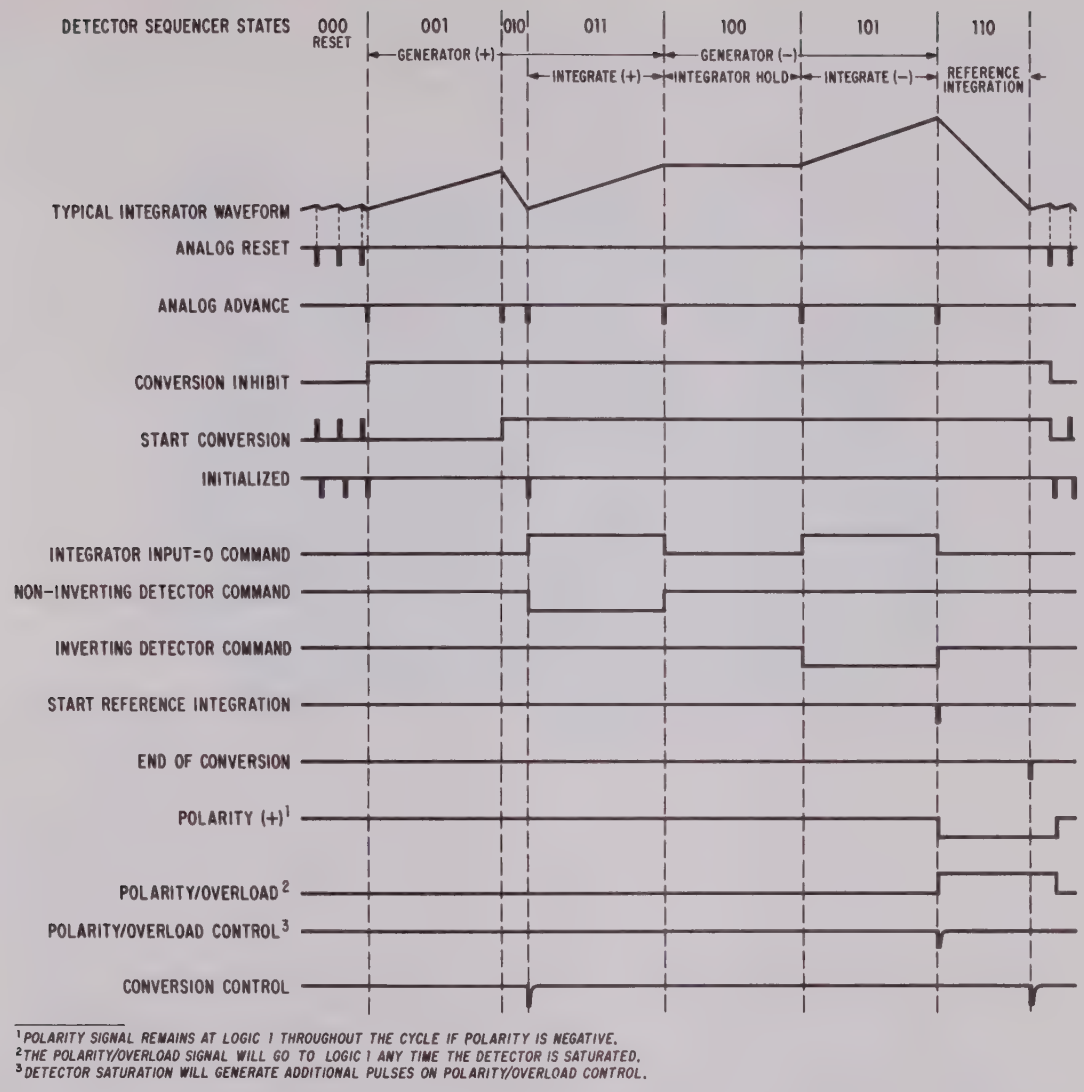


Figure 5-13. Detector Logic Block Diagram

Figure 5-14, the detector timing diagram, describes the operation of the detector logic in terms of its sequencing. The typical integrator waveform shown at the top of the diagram can be used as a kind of reference point when discussing the various states of the detector logic sequencer. This waveform is the result of the detector logic sequence. The reference integration shown on the far right is the result of the entire detector sequence.

The detector uses an integrator circuit (ESI Part No. 20909, see Figure 5-15) to obtain the algebraic difference of the two input voltages. The integrator operates like a standard integrating digital voltmeter. Prior to starting an integration cycle, the integrator must be given a command to drive the integrator output to a reference position. This signal is the start conversion signal shown on the timing diagram. The integrator is allowed to drift (no input connected to the integrator) when the system is either not operating or integrating on an input or reference voltage. To prevent the integrator from drifting to saturation in the reset state, an analog reset signal occurs at intervals of ≈3 ms. This signal is applied to the integrator in the same manner as a start conversion signal, except that a conversion inhibit signal is also applied during the reset state to prevent a full conversion cycle from being initiated.



[1] POLARITY SIGNAL REMAINS AT LOGIC 1 THROUGHOUT THE CYCLE IF POLARITY IS NEGATIVE.
[2] THE POLARITY/OVERLOAD SIGNAL WILL GO TO LOGIC 1 ANY TIME THE DETECTOR IS SATURATED.
[3] DETECTOR SATURATION WILL GENERATE ADDITIONAL PULSES ON POLARITY/OVERLOAD CONTROL.

Figure 5-14. Detector Timing Diagram

The detector sequence is generated by a counter on the detector logic assembly, which is advanced by the analog advance signal generated in the logic section of the Model 280. The logic signals that connect the detector section to the logic section - the analog advance signal, the analog reset signal, the polarity/overload control signal and the conversion control signal - are all transmitted through guarded pulse transformers. These pulse transformers, shown in Figure 5-17, maintain guarding and isolation integrity between the logic section and the detector section of the Model 280. A typical measurement sequence would proceed as follows: When the logic section of the Model 280 is signaled to start a measurement, it produces an analog advance signal to the detector section. When this signal is received in the detector, the detector sequencer is advanced by one count, which removes the conversion inhibit signal to the integrator. The detector remains in this state for ≈16 ms while the generator is allowed to settle on its first cycle. Another analog advance signal is then generated which advances the detector sequencer to a new state. At this point a start conversion signal is generated by the sequencer and applied to the integrator. The integrator responds in about 3 ms with an initialize signal. This signal is transmitted through the conversion control

transformer back to the sequencer in the main logic section of the Model 280, which is advanced one count. The logic section responds with another analog advance.

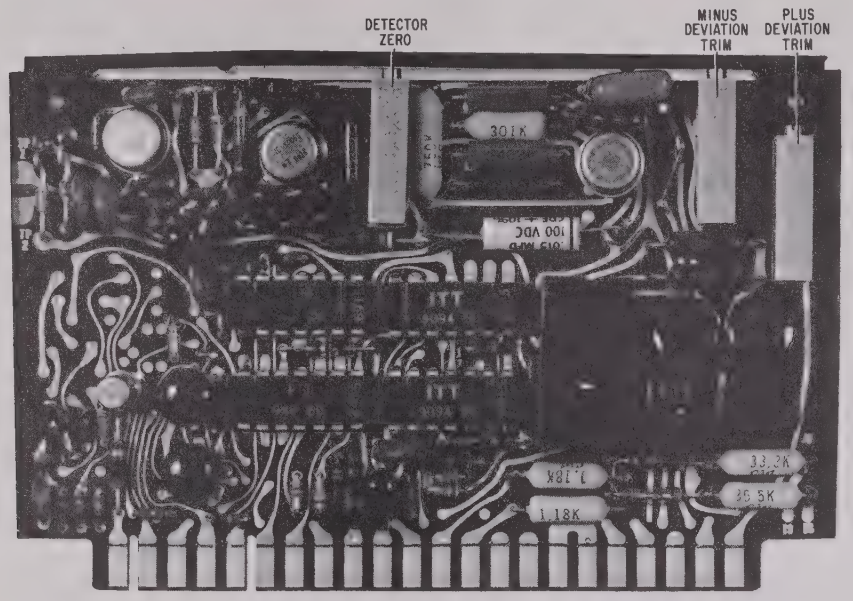
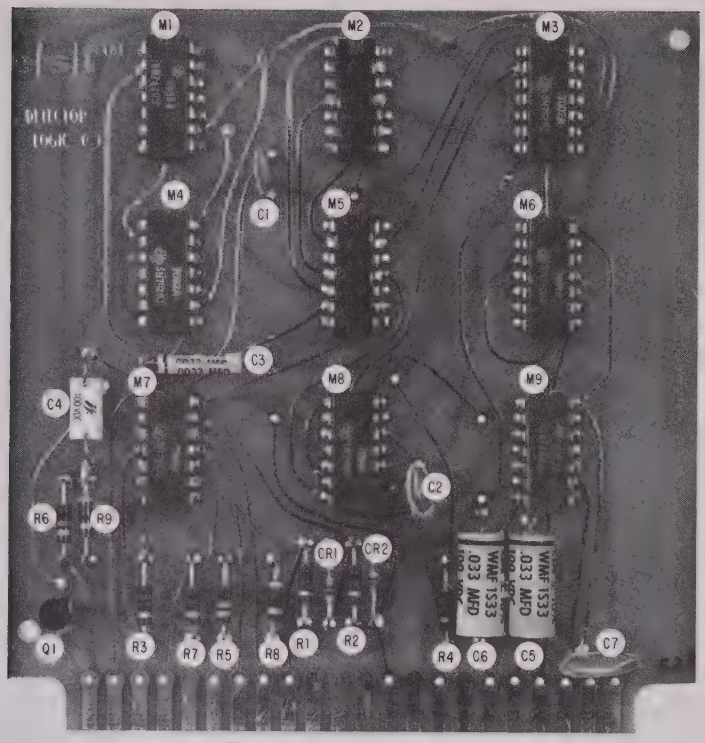


Figure 5-15. Integrator Assembly (20909)

The detector sequencer is now advanced to binary state 011. In this state the input of the integrator is connected through a non-inverting amplifier to the output of the bridge preamplifier signal for a period of 16 ms, after which another analog advance signal is received in the detector section. At this point the input to the integrator is connected to 0 volts, which in effect holds the integrator at a constant amplitude for another period of ≈16 ms while the generator is allowed to settle in the opposite polarity of the previous cycle.

Another analog advance pulse is received in the detector section, driving the detector sequencer to state 101. In this state the input to the integrator is connected through an inverting amplifier on the detector assembly to the output of the preamplifier. After this signal is integrated for 16.66 ms, a final analog advance pulse is received from the logic section. This advances the detector sequencer to the 110 state and at the same time connects a reference voltage to the integrator in place of the output from the preamplifier. This reference voltage is contained on the integrator circuit itself and is not part of the detector assembly. When the integrator has been driven back to the reference position by the integration of the reference voltage, an end conversion signal is transmitted by the conversion control transformer back through the guard to the logic section of the instrument. The logic section then responds by supplying analog reset signals to the detector section to put the detector in the reset state, ready for another measurement cycle.

Figure 5-16 is a schematic diagram of the detector logic assembly. The inputs and outputs are labeled to correspond to the signals shown in the detector logic block diagram (Figure 5-13) and the detector timing diagram (Figure 5-14). The internal gates are referred to in terms of row, column, and pin number. Above the schematic is a front view of the assembly, showing these rows and columns.



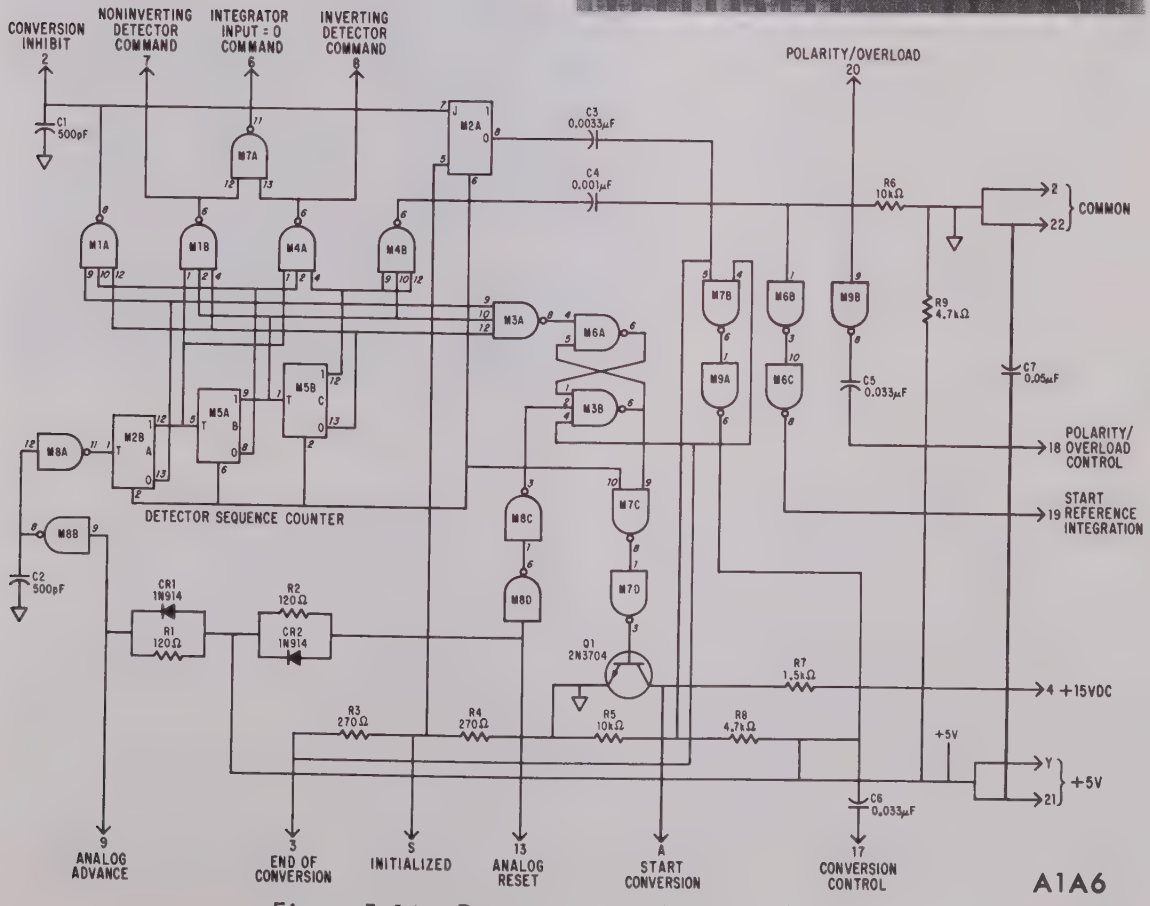
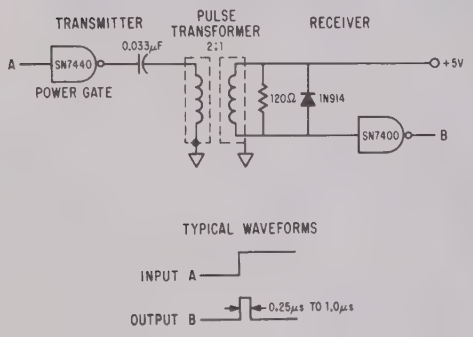


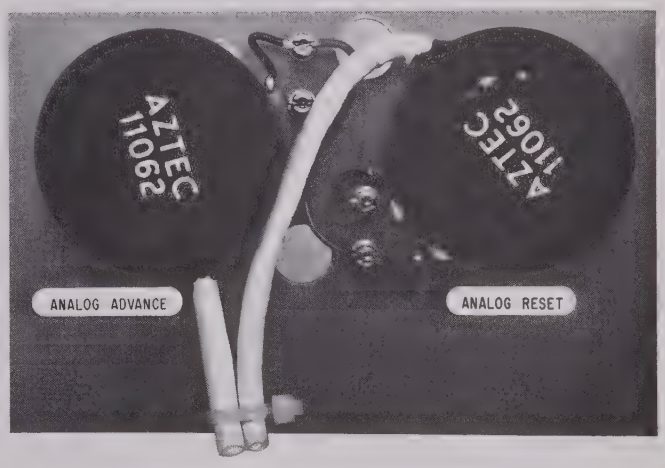
Figure 5-16. Detector Logic Assembly (19921)

The analog advance input and the analog reset input have special resistor/diode networks attached to them which provide terminating networks for transformers associated with these signals. The detector sequence counter is made up of flip-flop circuits on modules 0102 and 0202. The various sequencer states are decoded by gates located in modules 0101, 0301, and 0201. Special differentiating networks are provided at the output of flip-flop 0102 Pin 8 and the output of gate 0201 Pin 8. These networks are designed to develop a narrow pulse from the leading edge of the negative-going transition of the output of these two devices. Two 0.033 μF capacitors are attached to Pin 17 and Pin 18 on the detector logic assembly for ac coupling into the pulse transformers that transmit signals to the logic section. The outputs of gates 0303 Pin 8 and 0303 Pin 6 drive the transformers directly through these two capacitors. A special latch circuit (gates 0303 Pin 6 and 0103 Pin 6) provides a continuous start conversion signal once the start conversion pulse has been initiated. The start conversion signal can be reset (returned to the low state) by the end conversion signal from the integrator or by an analog reset pulse. The start conversion signal (not compatible with 5-volt logic) is the input to a unijunction transistor located in the integrator circuitry. It must be generated with a discrete transistor and a pullup resistor to + 15 volts dc.

5.2.2 Pulse Transformers

The pulse transformer diagram (Figure 5-17) shows the circuitry used to transmit pulses through the guard from analog-to-digital or digital-to-analog section of the Model 280.





A1T1, A1T2 and **A3T1, A3T2**

Figure 5-17. Pulse Transformer Circuitry

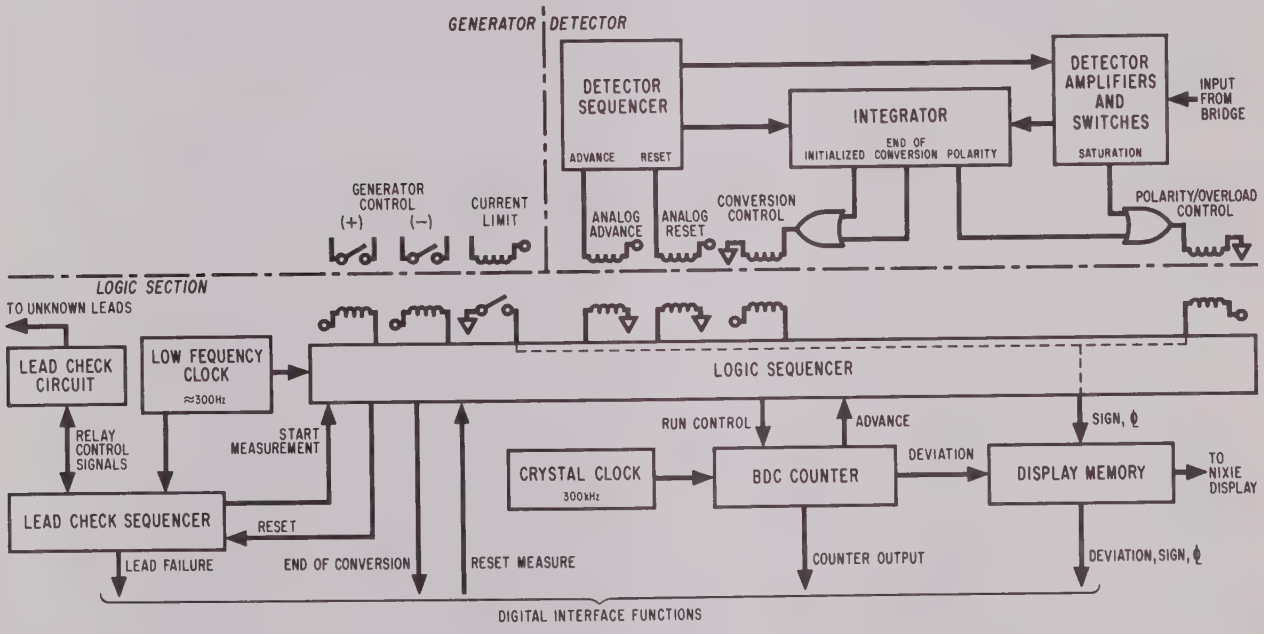
There are two transmitters and two receivers in the digital section of the Model 280 and two transmitters and two receivers in the analog section. The two transmitters in the digital section are the analog advance signal and the analog reset signal. The two transmitters in the analog (detector) section are the polarity overload control and the conversion control transmitters. The transmitting gate, an SN7440 power gate, drives the pulse transformer through a 0.033 μF capacitor. This provides dc coupling between the power gate and the transformer, necessary because the dc impedance of the transformer wiring is very low and puts excessive current drain on the power gate output in the true state. The receiving end of the pulse transformer is designed using a 120-ohm load resistor to approximate the transformer impedance and a 1N914 diode to clip all positive-going output of the pulse transformer. A standard SN7400 gate is used to accept the output of the transformer. The transformer turns ratio is approximately 2:1 to provide a good margin on the level of the signal at the transformer output. For a positive-going transition on the input to the power gate at point A, a signal ≈1/2 μs wide will be received at the output of the receiving gate, point B.

5.2.3 Logic Section

Figure 5-18, the logic block diagram and sequencer state table shows the major subsystems of the Model 280 logic. The major portion is in the logic section, with some logic in the detector (see Subsection 5.2.1). The measurement sequence is controlled by three separate sequencers and interconnecting logic. The sequencer state table indicates the relationship between the three sequencers.

NOTE

This table provides a means of correlating the various sections of the integrator waveform in the detector section. The detector timing diagram (Figure 5-14) shows the generator states associated with the various detector logic states.



CYCLE	LEAD CHECK SEQUENCER		LOGIC SEQUENCER		DETECTOR SEQUENCER	
	STATE FUNCTION	BINARY	STATE FUNCTION	BINARY	STATE FUNCTION	BINARY
START	RESET	000	RESET	0000	RESET	000
LEAD CHECK	SWITCH TO TERMINALS 1 AND 2	001	↕	↕	↕	↕
↕	CHECK TERMINALS 1 AND 2	010				
	SWITCH TO TERMINALS 3 AND 4	011				
	CHECK TERMINALS 3 AND 4	100				
LEAD CHECK	OPEN LEAD CHECK RELAYS	101	RESET	0000	RESET	000
MEASURE	MEASURE	110	TURN GENERATOR ON (+)	0001	REMOVE AUTOMATIC RESET	001
↕	↕	↕	RESET INTEGRATOR	0010	RESET INTEGRATOR	010
			INTEGRATE (+)	0011	INTEGRATE (+), MONITOR THE DETECTOR FOR ℄	011
			TURN GENERATOR ON (−)	0100	HOLD INTEGRATOR INPUT 0	100
			INTEGRATE (−)	0101	INTEGRATE (−)	101
			REFERENCE INTEGRATION	0110	REFERENCE INTEGRATION	110
			TRANSFER DATA	0111	RESET	000
			GENERATE CONVERSION COMPLETE	1000	↕	↕
MEASURE	MEASURE	110	GENERATE SYSTEM RESET	1001		
	RESET[1]	000	RESET	0000	RESET	000

[1] *IN CONTINUOUS CONVERSION ONLY THE LOGIC SEQUENCER IS RESET.*

Figure 5-18. Logic Block Diagram and Sequencer State Table

Figure 5-19 is a wiring diagram of the logic section of the Model 280. This drawing shows all interconnections between the input-output connectors J1 and J2, the logic assembly and the various assemblies that make up the logic section.

Figures 5-20 and 5-21 show the main part of the Model 280 logic section on a wire wrap assembly located in the bottom of the instrument. Figure 5-20 shows the logic sequencer, which directs the measurement cycle of the instrument and the lead check sequencer, which directs the lead check circuitry through its cycle. Figure 5-20 shows the binary-coded-decimal counter, which measures the various required system time delays and the reference integration time (which is proportional in magnitude to the deviation signal), and the display register or memory, consisting of 19 different flip-flops which hold the measurement results (deviation, polarity and overload signals) from the end of one measurement cycle until the end of the next. Primarily TTL gates and flip-flops are used on the wire wrap assembly, although some of the output functions, such as the display readout gates and the overload and polarity readout gates, are open collector DTL. All of the flip-flops are master-slave JK type. There are, however, many RS type latches formed of cross-coupled NAND gates. The locations of the gates are designated by a pair of numbers signifying a row and a column on the wire wrap assembly.

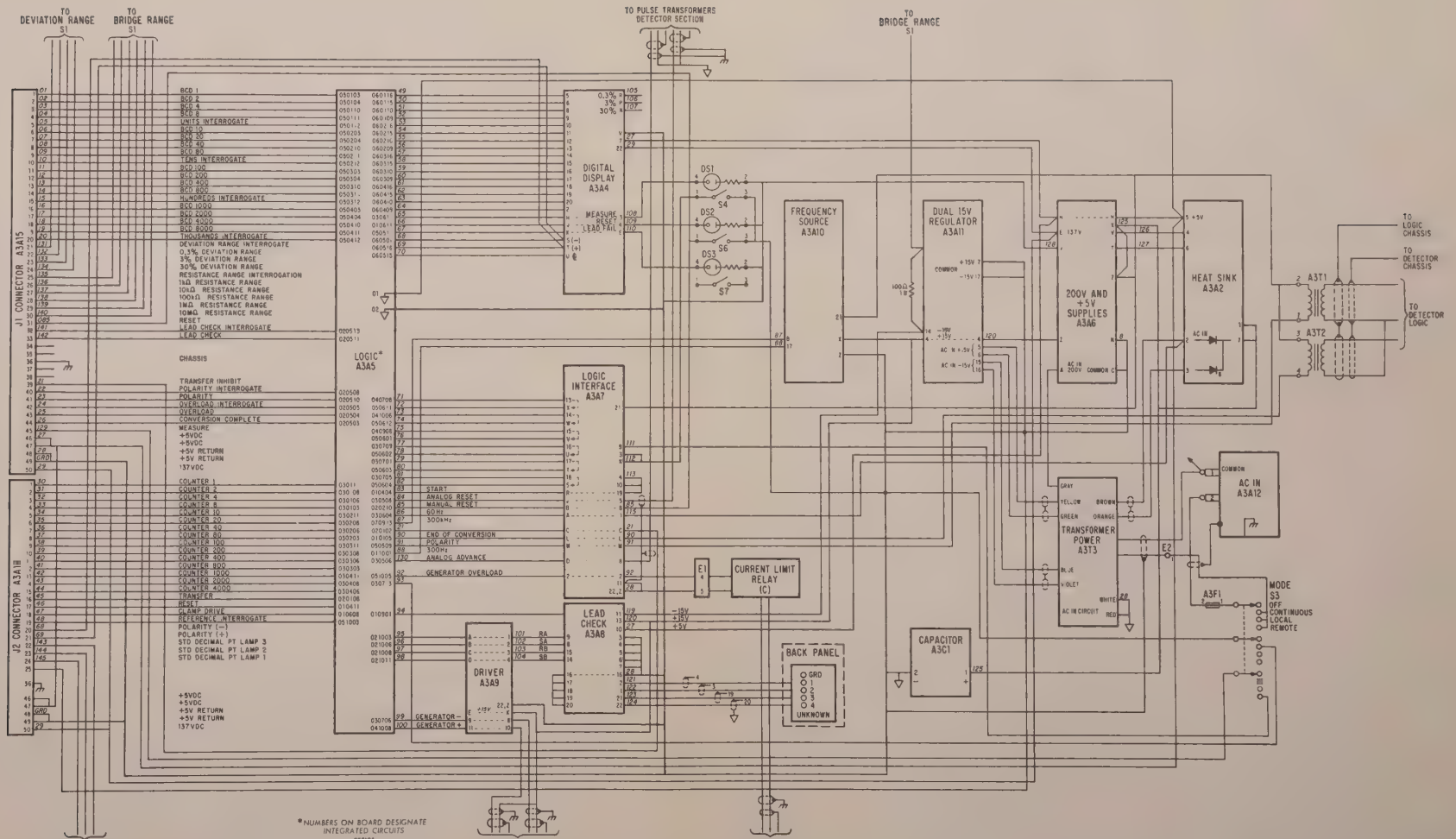


Figure 5-19. Logic Section Wiring Diagram

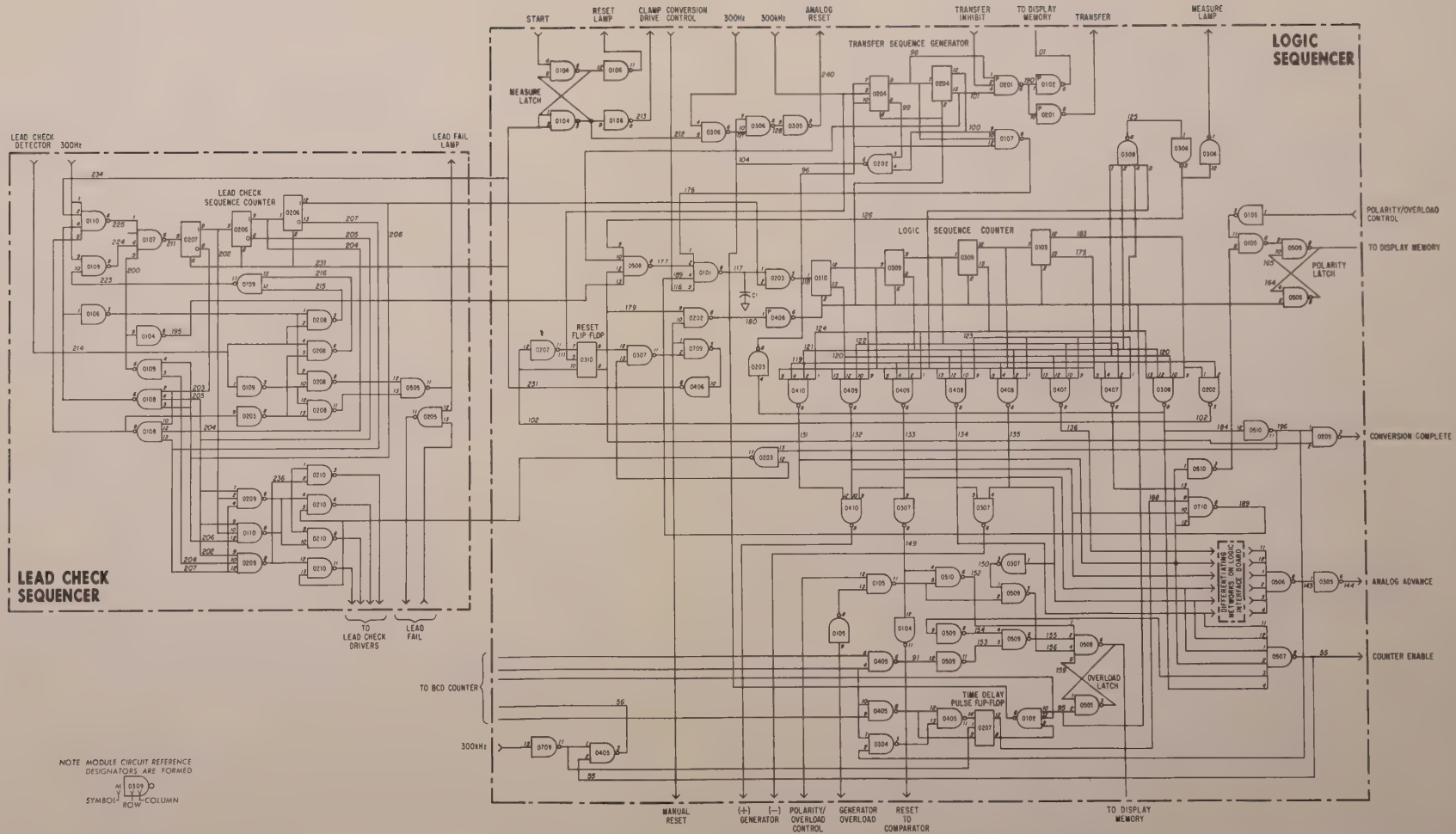
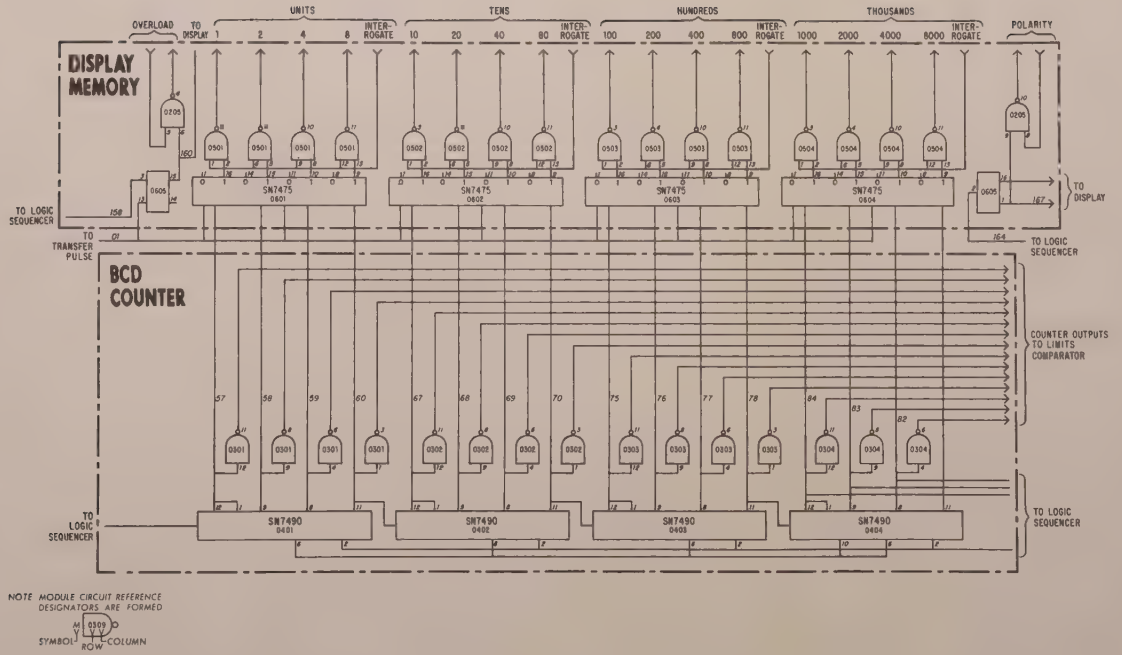
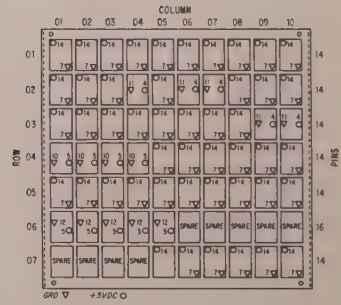
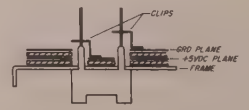


Figure 5-20. Logic Section Schematic Diagram (Part 1)



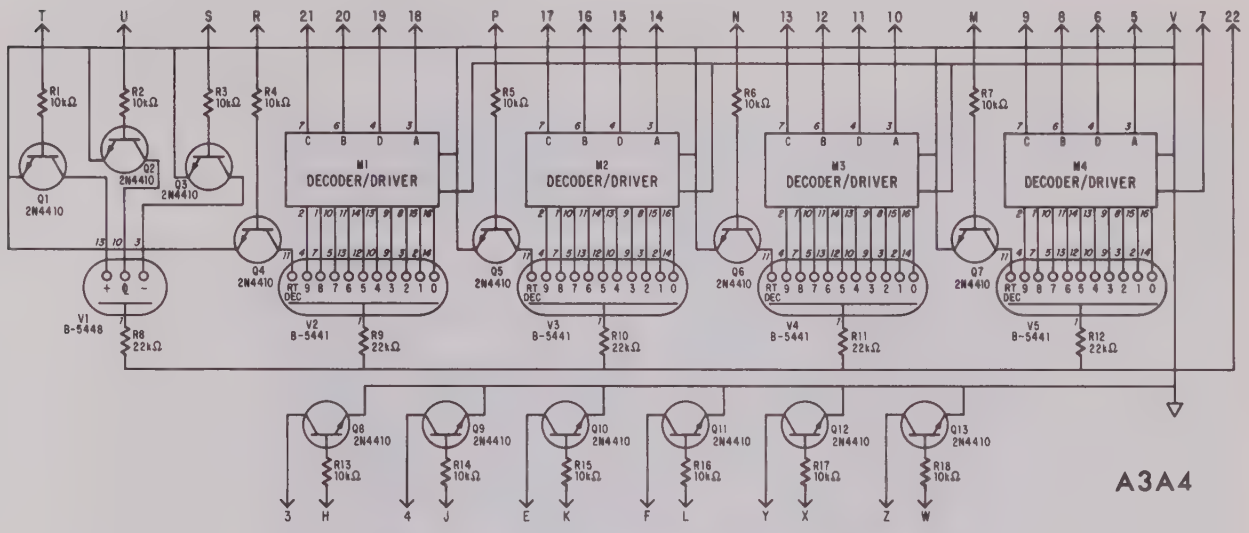




NOTE: THE LOGIC ONE (1) OUTPUTS FROM 0601, 0602, 0603 AND 0604 GO TO THE DISPLAY

Figure 5-21. Logic Section Schematic Diagram (Part 2)

Figure 5-22 is a schematic of the digital display assembly. This assembly contains the digital tubes, the high-voltage, decoder/drivers for these tubes, and an assortment of high-voltage transistors for driving other tube displays such as the Φ, +, -, •. Additional high-voltage drivers are provided for the neon indicators used on the front panel. This assembly may be unplugged and taken out through the front panel of the Model 280 Deviation Bridge for access to and service of these tubes and the driver circuitry.



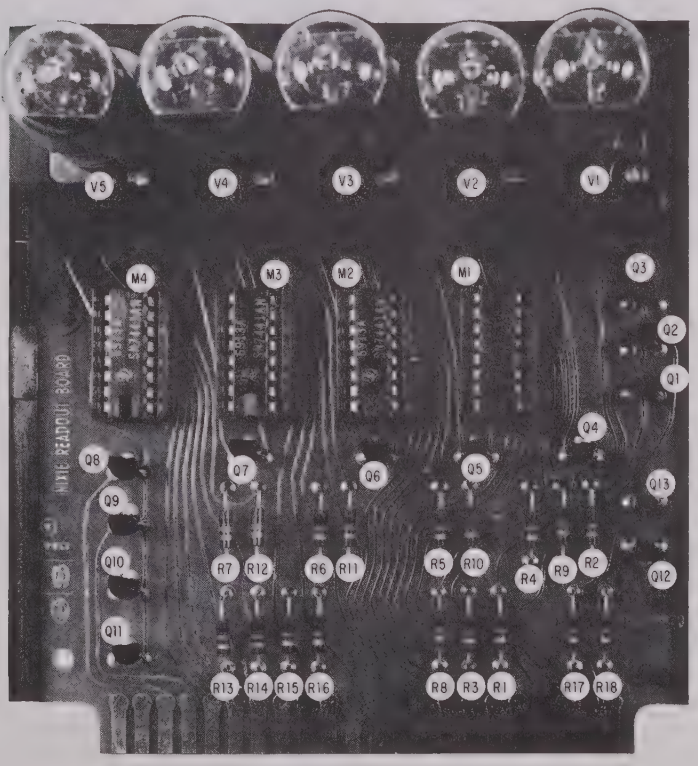
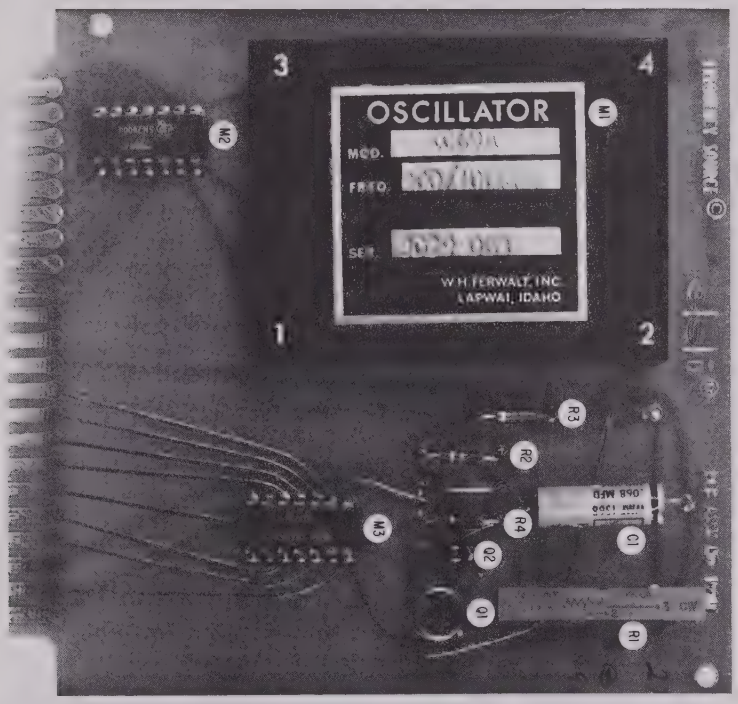


Figure 5-22. Digital Display Assembly (19870)

Figure 5-23 is a schematic of the frequency source assembly. This assembly contains two oscillator circuits, a crystal controlled 300 kHz and 100 kHz oscillator and a unijunction oscillator. The first oscillator has an internal divide-by-three circuit to produce 100 kHz. Gates are provided at the output to buffer the oscillator signals. The unijunction oscillator can be adjusted from ≈100 Hz to ≈1000 Hz. This frequency source is used to operate the lead check circuitry, while the high frequency source is used to derive the precise time intervals required for analog-to-digital conversions in the Model 280.



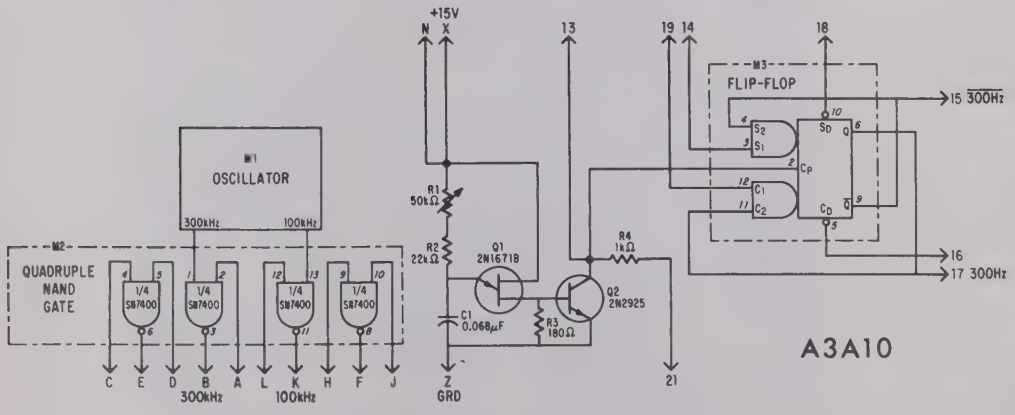


Figure 5-23. Frequency Source Assembly (19904)

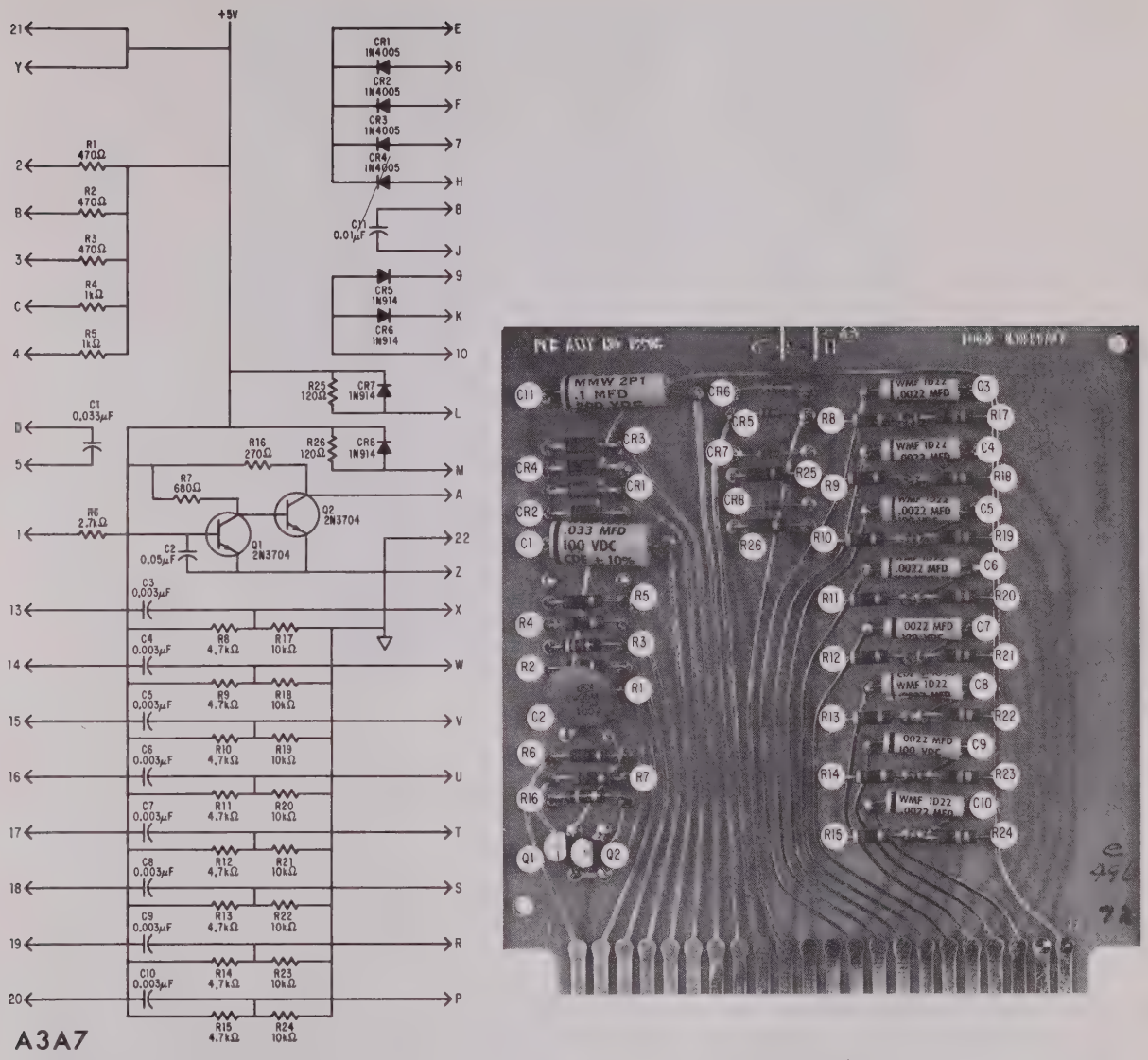


Figure 5-24. Logic Interface Assembly (19908)

Figure 5-24 is a schematic of the logic interface assembly. This assembly consists mainly of discrete-component circuitry used to augment the digital logic on the wire wrap assembly. Pullup resistors for use external to the logic assembly are provided on Pins 2, 3, 4, B, and C. Diode gate circuits are provided on Pins 6, 7, 9, 10, E, F, H and K. Capacitors are provided between Pins D and 5 and between Pins 8 and J. These are used as dc decoupling capacitors in the pulse transformer driver circuits. The circuits associated with Pins L and M terminate the pulse transformer circuits on the receiving end. The eight RC differentiating networks associated with inputs on Pins 13, 14, 15, 16, 17, 18, 19 and 20, are used in conjunction with logic internal to the wire wrap assembly to produce narrow pulses from leading edges of digital signals (see Figure 5-25). These circuits work on a negative-transition input. For example: A negative transition on Pin 13 would produce a narrow negative pulse output of 1/2 microsecond on Pin X. The 4 kΩ and 10 kΩ bias resistors are used to establish a voltage level at the output of the differentiating network compatible with the TTL gate circuit.

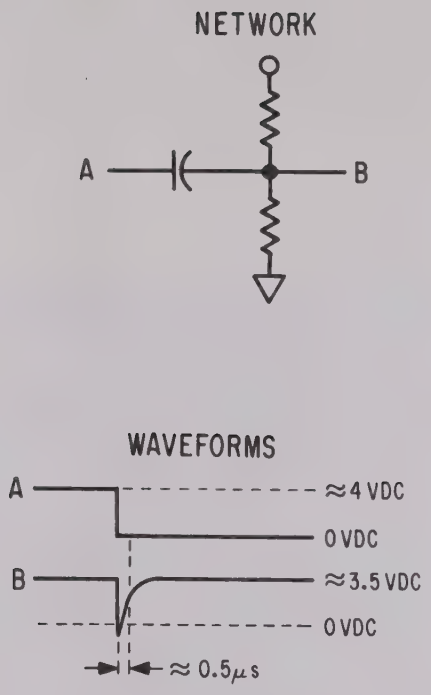
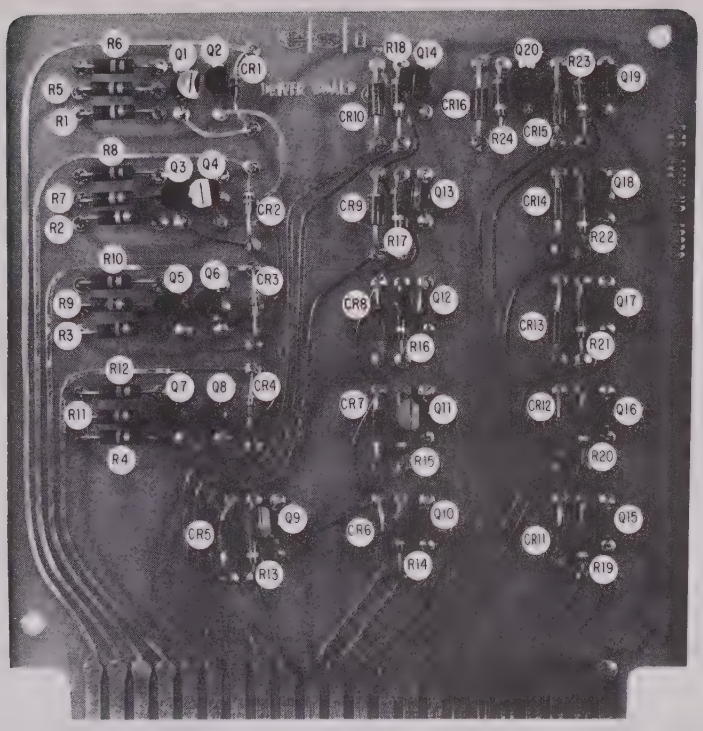


Figure 5-25. Differentiating Networks

Figure 5-26 is a schematic of the logic driver assembly. This assembly contains transitor driver networks used to drive high-level signals that are external to the digital logic assembly. The four circuits at the top of the drawing are non-inverting level-shifting driver circuits which drive the lead check relays on the lead check assembly. In the standard Model 280, only two of the remaining twelve driver circuits are utilized. The circuits with inputs on Pins 9 and 11 drive the polarity relays that program the polarity of the Model 280 generator. The remaining ten driver circuits are maintained as spares.



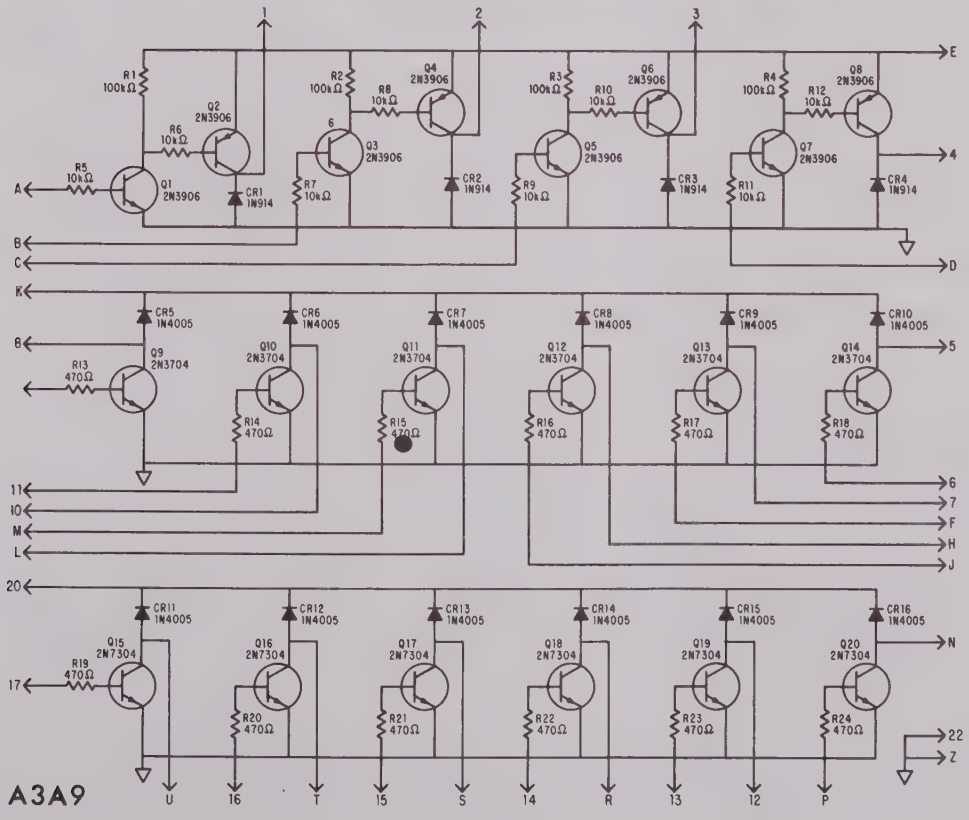
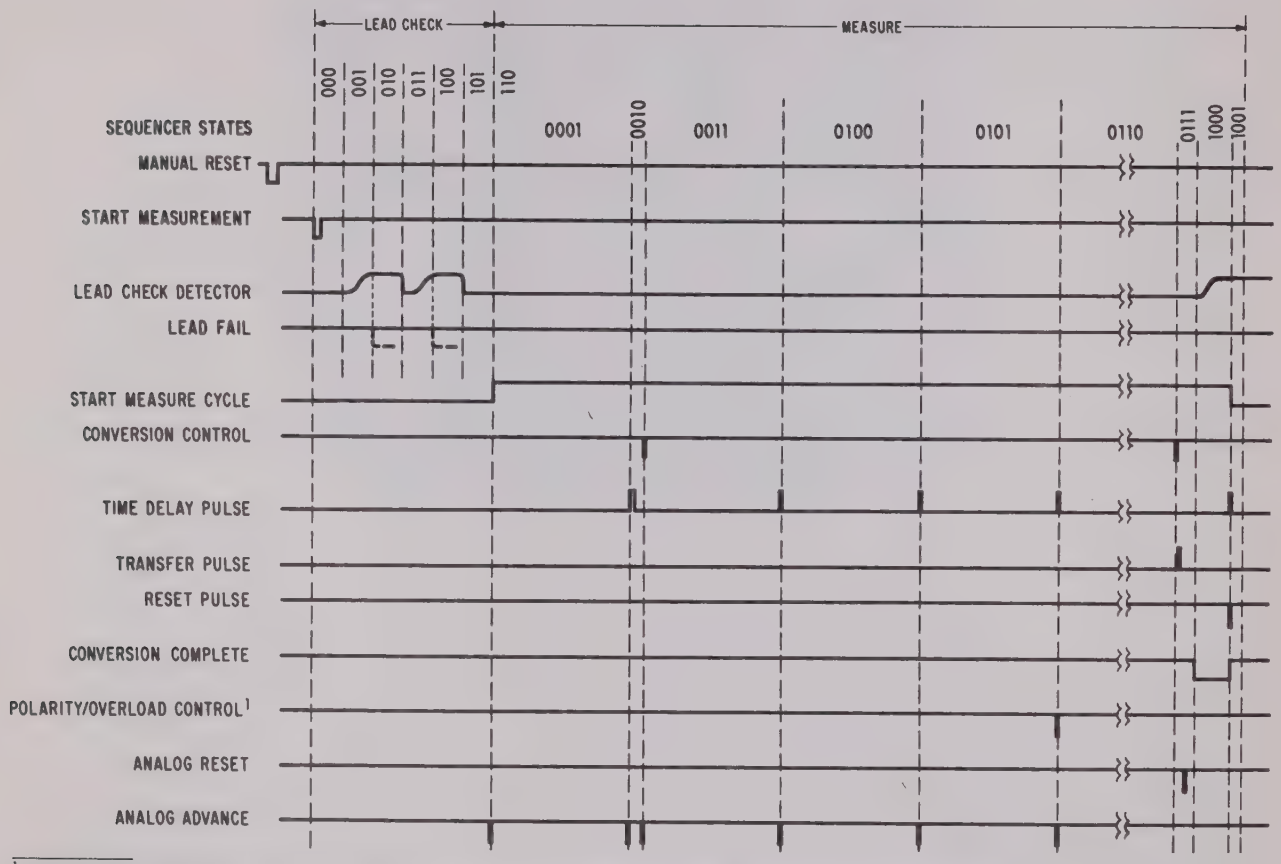


Figure 5-26. Logic Driver Assembly (19928)

5.2.4 Typical Measurement Cycle

The logic operation of the Model 280 is best described by following a typical measurement cycle. Figure 5-27 shows the timing of the Model 280 logic. (References to integrated



[1]PULSE SHOWN OCCURS ONLY FOR POSITIVE DEVIATION. DETECTOR SATURATION WILL GENERATE ADDITIONAL PULSES ON POLARITY/OVERLOAD CONTROL.

Figure 5-27. Logic Timing Diagram

circuit interconnection are shown in Figures 5-19 thru 5-21.) Only the first measurement in a group (after turning power on) must be preceded by a manual reset command, because an internal reset command is generated automatically following each measurement cycle. The logic diagram (Figures 5-20 and 5-21) shows that the manual reset command is applied to Pin 10, gate 0202 and Pin 1, gate 0709, producing a reset of the logic sequence counter, the polarity latch, the overload latch, the measure latch, the lead check sequence counter, the transfer sequence generator and the binary-coded-decimal counter. Thus a manual reset initializes the system.

Th next signal in the measurement cycle is a measure or start command, which sets the measure latch gate 0104, output on Pin 6, and gate 0104, output on Pin 3. The measure latch controls the reset lamp, the clamp drive signal and the automatic analog reset signal. When the measure latch (and thereby the system) is in the reset condition, the 300 Hz signal is connected to Pin 4 on gate 0306, and the output on Pin 6 is applied to the analog reset pulse

transformer, generating for each cycle an automatic analog reset command to the analog section of the instrument. Setting the measure latch applies a logic 1 on Pin 2 of gate 0110. This allows the lead check sequencer to begin operation when the next 300 Hz pulse occurs. The actual start command that appears at the input to the measure latch is ac coupled through a differentiating network on the logic interface board. Therefore a negative transition from an external source or from the front-panel MEASURE button will cause a pulse of ≈0.5 μs to be introduced into the measure latch.

LEAD CHECK SEQUENCER	
STATE FUNCTION	BINARY
RESET	000
SWITCH TO TERMINALS 1 AND 2	001
CHECK TERMINALS 1 AND 2	010
SWITCH TO TERMINALS 3 AND 4	011
CHECK TERMINALS 3 AND 4	100
OPEN LEAD CHECK RELAYS	101
MEASURE	110
↕	↕
MEASURE	110
RESET[1]	000

[1]IN CONTINUOUS CONVERSION ONLY THE LOGIC SEQUENCER IS RESET.

Figure 5-28. Lead Check Sequencer State Table

The lead check sequencer states are shown in Figure 5-28. The first operation in the lead check cycle is the connection of the lead check circuitry to bridge UNKNOWN terminals 1 and 2. The lead check sequencer logic decodes the state of the lead check sequence counter and applies a corresponding signal to the drivers (on the driver assembly) which operate the lead check latching relay. This signal is applied for approximately 1 cycle of 300 Hz or ≈3.3 ms. At the next 300 Hz pulse, the lead check circuitry samples the output of the lead check detector circuit. If the lead check shows a failure, the lead fail output will go to a logic 0 and the LEAD FAIL lamp will light. If the continuity between UNKNOWN terminals 1 and 2 is satisfactory, the instrument will proceed on the next 300 Hz clock pulse to connect the lead check detector to UNKNOWN terminals 3 and 4 and disconnect it from terminals 1 and 2. At the occurrence of the next 300 Hz clock pulse, the logic samples the output of the lead check detector again. If the output is not acceptable, the lead fail output will go to a logic 0 and the LEAD FAIL lamp will light; if it is acceptable, the next 300 Hz clock pulse will cause the lead check relay to return to a normal position, not connected to any of the UNKNOWN terminals. The next 300 Hz clock pulse causes the lead check sequencer to advance to state 110, which issues a start measurement cycle pulse to the logic sequence

counter. The lead check sequencer then remains in this state (110) until the end of the measurement cycle. If a lead failure does occur when the lead check logic samples the output of the lead check detector, the instrument will not proceed beyond that point; the lead check has to be satisfactory or the bridge will not continue. If, however, the lead connection does become satisfactory, the lead check detector output will go to the proper state and the next 300 Hz clock pulse will advance the lead check circuit to its next sequential state. When the lead check sequencer transfers to state 110, the output of gate 0104 Pin 8 goes to a logic 0. This logic 0 goes to gate 0508 in on Pin 13, through gate 0101 in on Pin 2, through gate 0203 in on Pin 1 and advances the logic sequence counter one count to state 0001. The output of gate 0410 Pin 6 goes to logic 0. This logic 0 is applied to gate 0507 Pin 2, which allows the BCD counter to start running. At the same time the output from gate 0410 Pin 6 is applied through a differentiating network to Pin 12 of gate 0506 to provide an analog advance signal to the detector section of the instrument. The BCD counter is now running at a 300 kHz rate and a time interval is being measured out.

LOGIC SEQUENCER		DETECTOR SEQUENCER	
STATE FUNCTION	BINARY	STATE FUNCTION	BINARY
RESET	0000	RESET	000
↕		↕	↕
RESET	0000	RESET	000
TURN GENERATOR ON (+)	0001	REMOVE AUTOMATIC RESET	001
RESET INTEGRATOR	0010	RESET INTEGRATOR	010
INTEGRATE (+)	0011	INTEGRATE (+), MONITOR THE DETECTOR FOR ϕ	011
TURN GENERATOR ON (−)	0100	HOLD INTEGRATOR INPUT 0	100
INTEGRATE (−)	0101	INTEGRATE (−)	101
REFERENCE INTEGRATION	0110	REFERENCE INTEGRATION	110
TRANSFER DATA	0111	RESET	000
GENERATE CONVERSION COMPLETE	1000	↕	↕
GENERATE SYSTEM RESET	1001		
RESET	0000	RESET	000

Figure 5-29. Logic Sequencer and Detector Sequencer State Tables

At the time the logic sequencer entered the 0001 state (see Figure 5-29), the output of gate 0410 Pin 8 was driven to a positive (logic 1). This signal, applied to the relay driver circuitry actuates the relay that turns the generator on in the positive direction. A time delay allows the generator to settle to final value in this polarity. When the BCD counter reaches 5000 counts (after 16.66 ms) the time delay pulse flip-flop 0207 input on Pin 1 is set for one period of 3.3 microseconds. Its one output is fed back through gate 0310 Pin 9, through gate 0101 Pin 4, through gate 0203 Pin 1 into the logic sequence counter, advancing the counter by one more count at the end of the 16.66-ms period and putting the sequencer into the 0010 state. The sequencer generates another analog advance signal, which is transmitted through the guarded pulse transformers to the detector section. The detector responds with a pulse on the conversion control input. This pulse advances the logic sequence counter to the 0011 state

which generates another analog advance signal to the detector section. With the logic sequence counter in the 0011 state, the first unknown integrate cycle is performed and the counter is measuring out another 5000 counts or a period of 16.66 ms. At the end of this period the time delay pulse flip-flop generates another advance pulse to the logic sequence detector section and the generator polarity is reversed: the output of gate 0410 Pin 8 goes back to a low and the output of gate 0307 Pin 6 goes to a high. The output of gate 0307 Pin 6 goes directly to the minus polarity relay driver which selects the minus polarity relay in the generator section of the instrument. The BCD counter is measuring out another 16.66 ms period, to allow the generator to settle in the opposite polarity, after which the time delay pulse flip-flop generates another advance signal to the logic sequence counter. The logic sequence counter advances to state 0101, generating another analog advance signal to the detector section. The second integrate cycle is then performed on the detector signal. The BCD counter again measures out 16.66 ms and another advance signal is then generated by the time delay pulse flip-flop to the logic sequence counter, putting the logic sequencer in the 0110 state. Another analog advance signal is generated to the detector section.

The detector now starts reference integration. If the polarity of the unknown signal is positive, a pulse will occur on the polarity overload control transformer which will set the polarity latch to indicate a positive polarity. The sequencer will be advanced by a pulse on the conversion control line signifying that the integrator has detected zero crossing and that the time interval that represents the voltage stored in the integrator has now elapsed. When the sequencer advances from state 0110 to 0111, the number of counts that occurred during the 0110 state will be stored in the BCD counter.

At this point the sequencer enters a subsequence that transfers the data from the BCD counter into the display memory and generates a special reset signal to the analog section and another advance signal to the logic sequence counter. To accomplish this subsequence, flip-flops 0204 input on Pin 5 and 0204 input on Pin 1 are used. This is designated a transfer sequence. As soon as the logic sequence counter enters the 0111 state, a logic 1 is applied to Pin 7 and Pin 10 inputs of module 0204. The next 300 kHz clock pulse sets flip-flop 0204 input on Pin 5 generating a logic 1 on the transfer inputs to the display latches (display memory flip-flops). This signal remains true (logic 1) for one period of 300 kHz. The transfer sequence generator is advanced by one more count, the output of gate 0202 on Pin 6 is driven to a ground (logic 0) which provides a logic 0 output to the analog reset transformer, generating an analog reset pulse in the detector section. The next 300 kHz clock pulse advances the transfer sequence generator one more state and generates an advance pulse to the logic sequence counter in gate 0107 output on Pin 8.

The logic sequence counter is now advanced to state 1000, which is the conversion complete state. In this state a logic 0 is generated at the output of gate 0205 Pin 3 which is the conversion complete signal. The BCD counter is allowed to run during this period of time. However, the time delay pulse flip-flop is set at 1000 counts instead of 5000 counts, so that the logic sequence counter will be advanced to a new state, the reset state (1001), at 3-1/3 milliseconds. In this state a logic 1 is applied to the reset flip-flop input on Pin 7 and a logic 0 is applied to the reset flip-flop input on Pin 10. This will allow the reset flip-flop to set on the next 300 kHz clock pulse, and a logic 0 will be applied to the reset inputs on the logic sequence counter, the transfer sequence generator, the polarity latch, and the overload latch, and, unless the instrument is in the continuous conversion mode, a reset will also be applied to the measure latch and the lead check sequence counter. In the continuous conversion mode the input on Pin 13 on gate 0307 inhibits the reset signal from being applied to the lead check sequence counter and the measure latch so that the instrument will start another measure cycle without performing a lead check or requiring another measure signal input.

Gate 0203 provides a unique function during the conversion cycle. If the instrument is not in the continuous conversion mode, the 3.3 ms time period that is used to generate the conversion complete signal is also applied to the lead check relay circuitry. This provides a means of closing the lead check relays across the bridge terminals to prevent possible damage to the bridge in the reset mode. The MEASURE lamp control signal is derived from the reset state of the logic sequence counter so that any time the logic sequence counter is not in the reset state the MEASURE lamp will be on.

The overload signal can be generated by any of three conditions: If the generator current limits, if the number of counts in the reference integration exceeds 3000, or if detector saturation occurs. The inputs on gate 0105 on Pins 12 and 13 indicate the detector saturation and the generator overload signals, respectively. The generator overload is coupled through a guarded relay located in the logic section of the instrument and driven from the detector section. This relay should normally be closed, a logic 0 or contact closure to ground on the Pin 9 of gate 0105 indicating that the generator is not overloaded. This will generate a logic 1 into Pin 13 on gate 0105. If either Pin 12 or Pin 13 of gate 0105 is driven to a ground during the integrate cycles, the output of gate 0105 will be sampled by gate 0510 input on Pin 5 and gate 0509 input on Pin 2. If gate 0105 Pin 11 goes to a logic true during one of the two integrate cycles, a logic 0 is generated on either Pin 1 or Pin 4 of gate 0508. This will set the latch that is composed of gate 0508 output on Pin 6 and gate 0505 output on Pin 3 which provides an input to the overload display memory flip-flop (gate 0605 input on Pin 3). When the transfer pulse occurs, the display memory flip-flop will indicate an overload. The polarity/overload control signal that comes into gate 0105 on Pin 12 is time-shared (multiplexed) between the signal that indicates detector saturation and the signal that indicates the polarity. However, the polarity flip-flop latch samples this signal only during the reference integration cycle, and the overload latch is effectively sampling the signal only during the unknown integration cycles. The overload caused by too large a signal (the number of counts exceeding the limit) is detected by decoding 3000 counts in gate 0405 output on Pin 6 from the BCD counter during the reference integrate cycle.

5.3 GUARDED REED RELAYS

5.3.1 Current Limit Relay

The contacts of the current limit relay will be open when the Model 280 generator is current limited (overloaded) and will be closed when the generator is voltage regulating. For a complete description of the operation of the current limit relay, see Paragraph 5.1.7 (Generator and Bridge).

If a Model 280 indicates a measurement overload when it should not, or cannot be aligned as described in Paragraph 3.3.3 (Generator Current Alignment), then the current limit relay should be tested as follows:

1. Using BRIDGE RANGE kΩ3 and DEVIATION RANGE 3%, measure a 100 kΩ resistor. Balance Model 727 for minimum possible deviation.

2. Set Model 280 MODE switch to CONTINUOUS and push the MEASURE button.

3. Connect an oscilloscope to the switch terminals of the current limit relay.

WARNING

The current limit relay is located next to the 110 V power line wiring. This high voltage can cause serious injury or death.

4. Observe the voltage waveform on the current limit relay terminals. There should be zero voltage difference except when the generator polarity is reversed once every 33 milliseconds. Every 33 milliseconds there should be a 1- or 2-millisecond period during which the voltage difference between the relay terminals will be 5 volts or zero volts (relay bounce is observable during this period). The transitions between 5 volts and zero volts should be sharp and clean.

5.3.2 Generator Control Relays

One of the generator control relays will be actuated for each generator output polarity. Neither is actuated when the generator is off. They are never actuated simultaneously. For a complete description of the operation of the Generator Control Relays, see Paragraph 5.1.7.

When the generator control relays are actuated, they make connections between edge connector pins on the generator reference and current limit assembly as follows:

Generator Output Positive	Generator Output Negative
X to T	X to R
D to R	D to T
P to C	P to A

If a Model 280 is not working properly and the logic section does not seem faulty, the generator control relays should be checked as follows:

1. Remove all five boards from the generator section of the Model 280.

2. Turn the Model 280 on and push the RESET button.

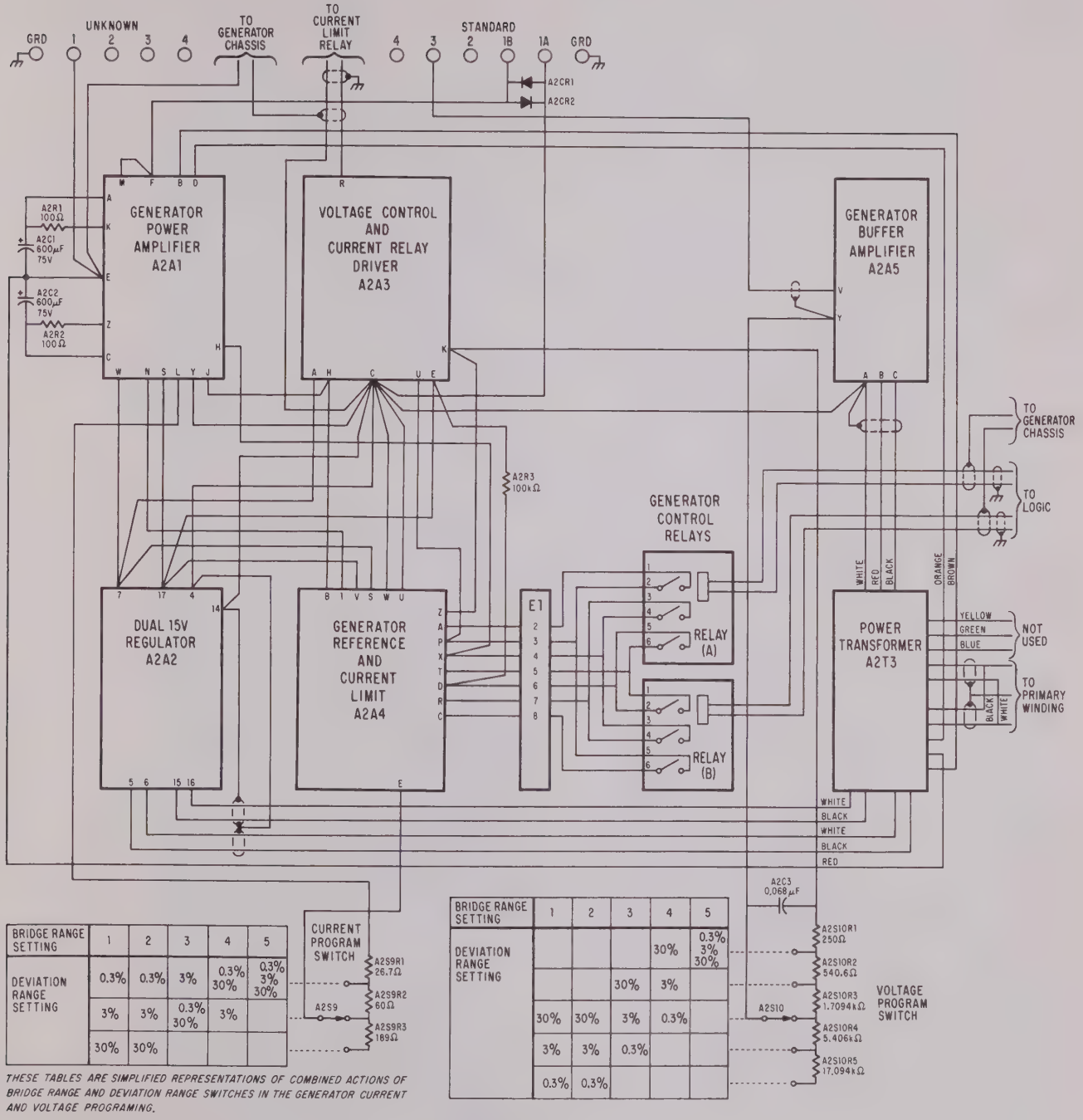
3. Swing the logic plane out (as described in Section 6.1) and connect a jumper from Pin 22 to Pin 8 on the driver board.

4. Using an ohmmeter, check to see that one of the generator control relays is actuated and that each of the three switch resistances is less than one ohm. As each switch is checked, operate it several times to be sure that it is consistant.

5. Move the jumper from Pin 8 to Pin 10 on the driver board. Leave the other end of the jumper tied to Pin 22.

6. Using an ohmmeter, check to see that the other generator control relay is actuated and that each of the three switch resistances is less than one ohm. As each switch is checked, operate it several times to be sure that it is consistant.

5.4 WIRING DIAGRAMS



BRIDGE RANGE SETTING	1	2	3	4	5
DEVIATION RANGE SETTING	0.3%	0.3%	3%	0.3% 30%	0.3% 3% 30%
	3%	3%	0.3% 30%	3%	
	30%	30%			

BRIDGE RANGE SETTING	1	2	3	4	5
DEVIATION RANGE SETTING				30%	0.3% 3% 30%
			30%	3%	
	30%	30%	3%	0.3%	
	3%	3%	0.3%		
	0.3%	0.3%			

THESE TABLES ARE SIMPLIFIED REPRESENTATIONS OF COMBINED ACTIONS OF BRIDGE RANGE AND DEVIATION RANGE SWITCHES IN THE GENERATOR CURRENT AND VOLTAGE PROGRAMING.

Figure 5-30. Generator Section Wiring Diagram

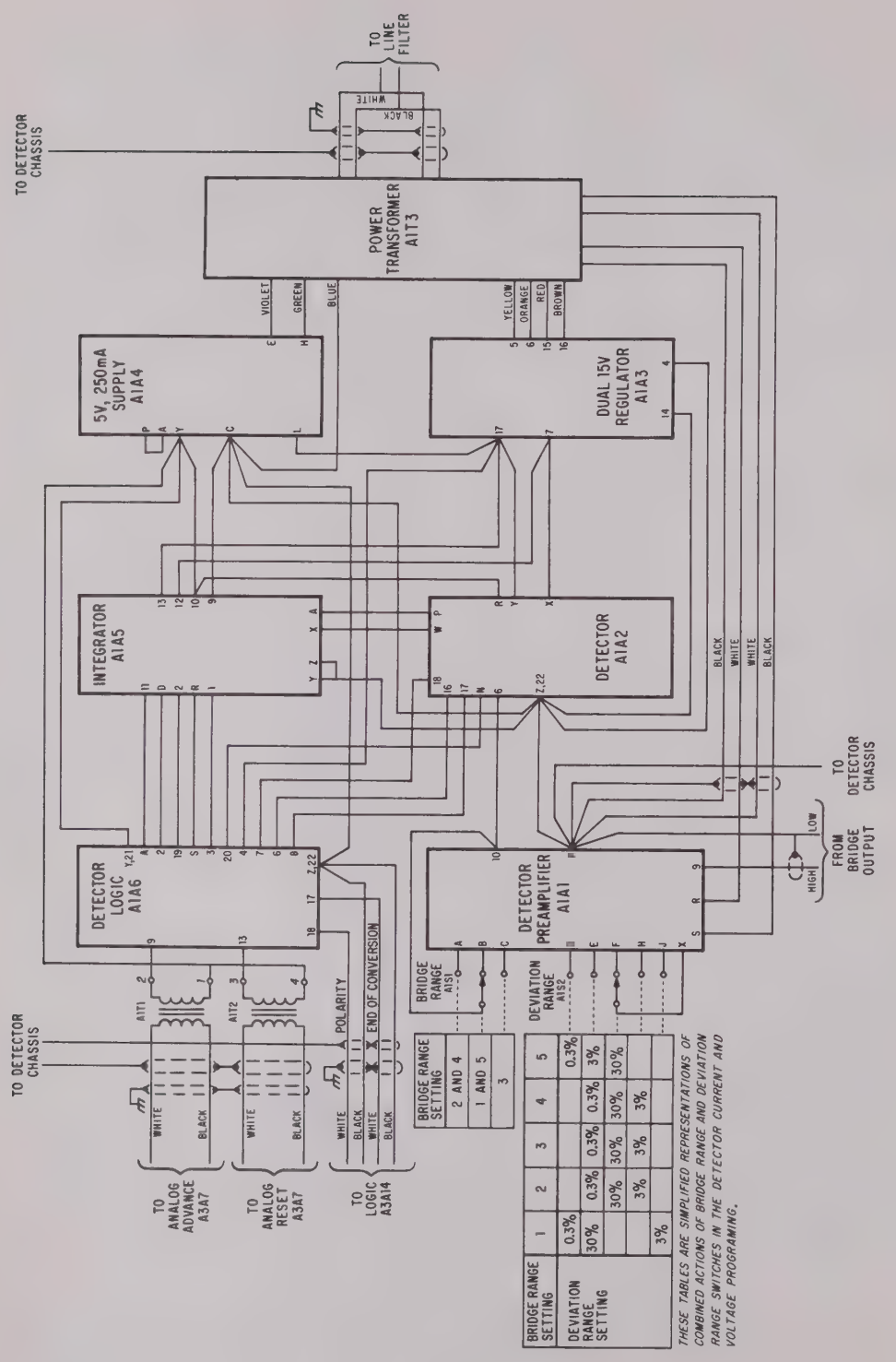


Figure 5-31. Detector Section Wiring Diagram

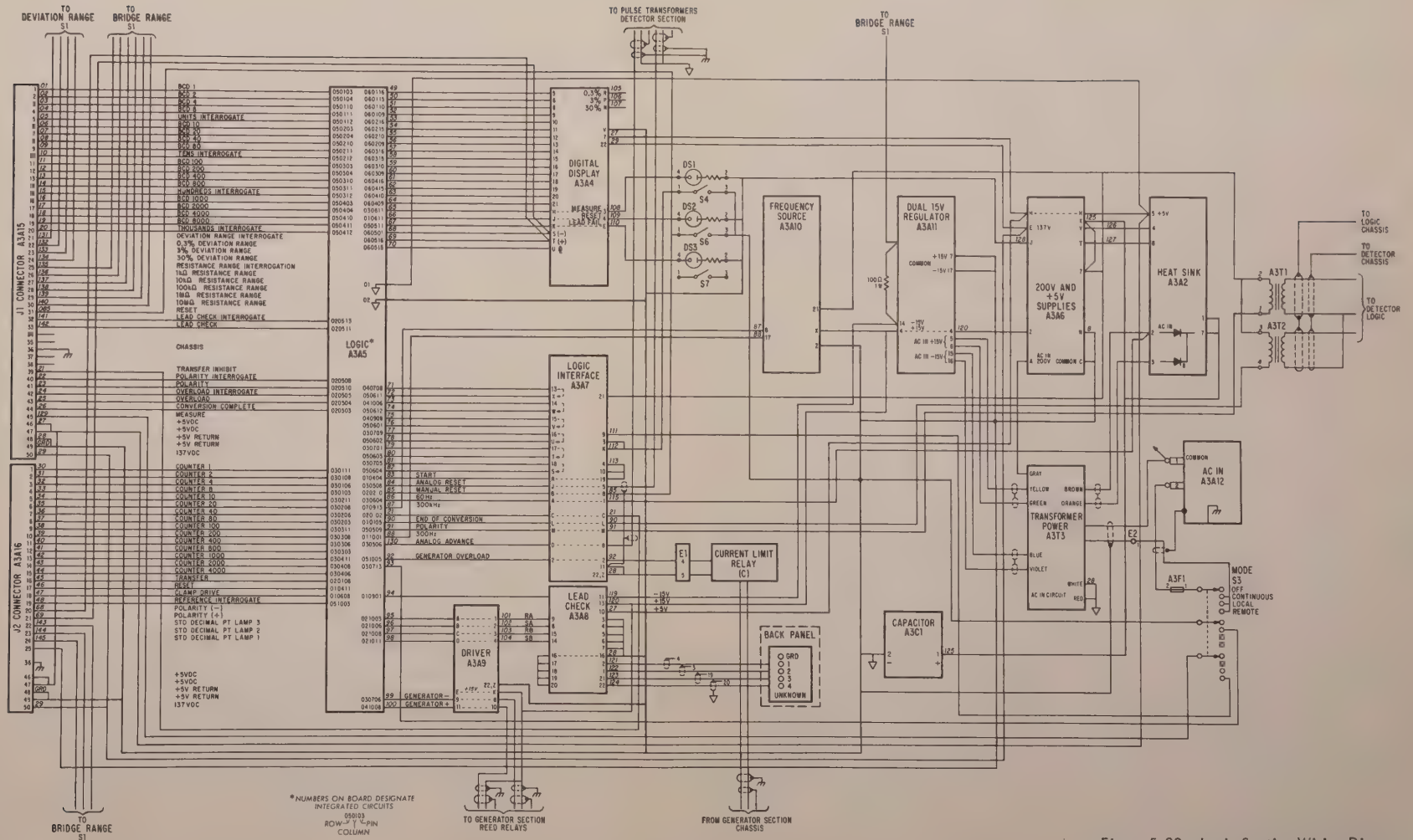


Figure 5-32. Logic Section Wiring Diagram

SECTION VI

MAINTENANCE AND REPAIR

6.1 ACCESSING COMPONENTS

Prepare a soft, clean place to set the instrument. Be sure that no projections or pointed objects will be underneath it and that there are no metal filings in the area.

To remove the Model 280 from the cabinet, remove the four mounting screws (one in each corner of the front panel), disconnect all connections to the bridge, then slide the unit out the front of the cabinet as far as possible. Push the release clip on each of the metal tracks and remove the unit. Place on prepared surface.

To remove the top or bottom dust cover, release the quarter-turn fasteners on that cover and lift it off. To access circuit assemblies in the generator or detector subassembly, remove the screw on the cover and lift. To access the logic plane, remove two screws nearest the rear of the unit.

6.2 PERIODIC MAINTENANCE

The following procedures should be performed approximately once a year to insure maximum accuracy and reliability from the Model 280 Deviation Bridge. If problems can be isolated to individual circuit assemblies, the defective assembly should be returned to the factory for repair or replacement. If the need for major repairs is apparent, it is recommended that the unit be sent to the factory for service. If you are unable to release the unit, the service department will be happy to furnish the necessary information and replacement parts. Unauthorized repairs, however, will invalidate the instrument warranty.

6.2.1 Visual Inspection

Inspect the outside of the unit for dial orientation and damage to connectors, binding posts and binding post caps. Check for dirt around the binding post insulators.

Inspect the interior for loose or broken connections, damaged or dirty switch or socket contacts, heat-damaged resistors and resistors touching each other or the grounded switch structure.

6.2.2 Cleaning and Lubrication

Clean the front panel with a soft, dry, lint-free cloth, being particularly careful to remove all dirt from around binding post insulators.

The only internal components that may require maintenance are the rotary switches. These are carefully lubricated at the time of manufacture and are protected by the instrument case. They should rarely, if ever, require maintenance. It is recommended that they be cleaned and lubricated *only* if they are not making good electrical contact. Proceed as follows:

1. Place instrument horizontally on bench, with a sheet of white paper under switch to be cleaned. Spray switch with Freon TF degreaser in aerosol can (Miller Stephenson Co. or equivalent) until no more dirt appears on paper. Drying is not necessary.

2. Lubricate with a low-conductivity oil (Viscosity Oil Co., No. 7069, available from ESI as Part No. 13500). Apply one drop to each rotor tab and one drop to the rotor ring contact, using a hypodermic needle. With a small brush, apply a dab of petroleum jelly to each switch bearing and detent mechanisum. DO NOT OVERLUBRICATE.

6.3 REPAIR

6.3.1 Part Location

All circuit assemblies and chassis-mounted components are shown in Figures 6-1a and 6-1b. Figure 6-1a is a top view of those bridges with serial number 033001 and after. Figure 6-1b shows previous locations of pulse transformers and trimmers on bridges with serial numbers between 940001 and 940020.

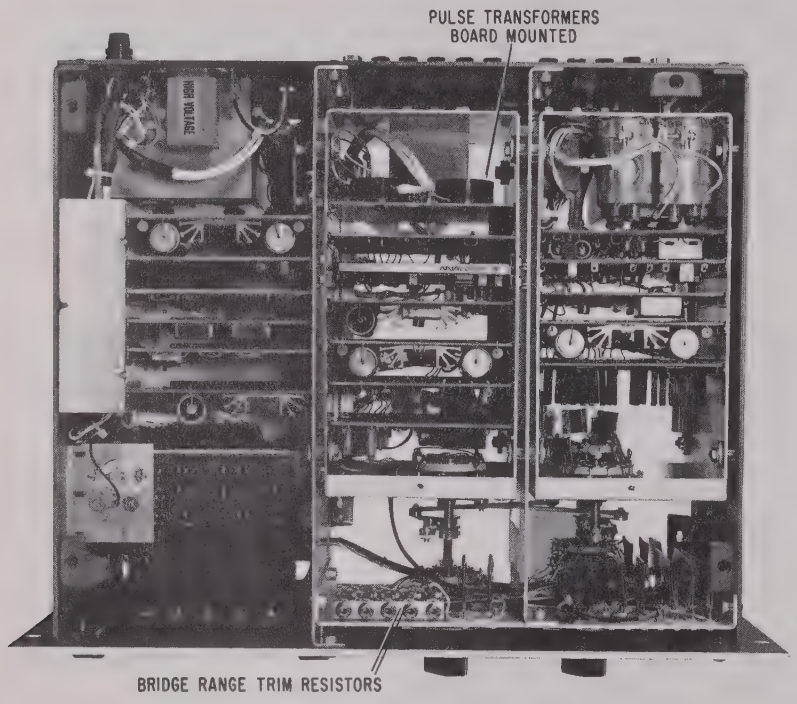


Figure 6-1a. Locations of Circuit Assemblies and Chassis-Mounted Parts (Serial Numbers 033001, etc)

Figure 6-1b. Relocated Parts (Serial Numbers 940001 thru 940020

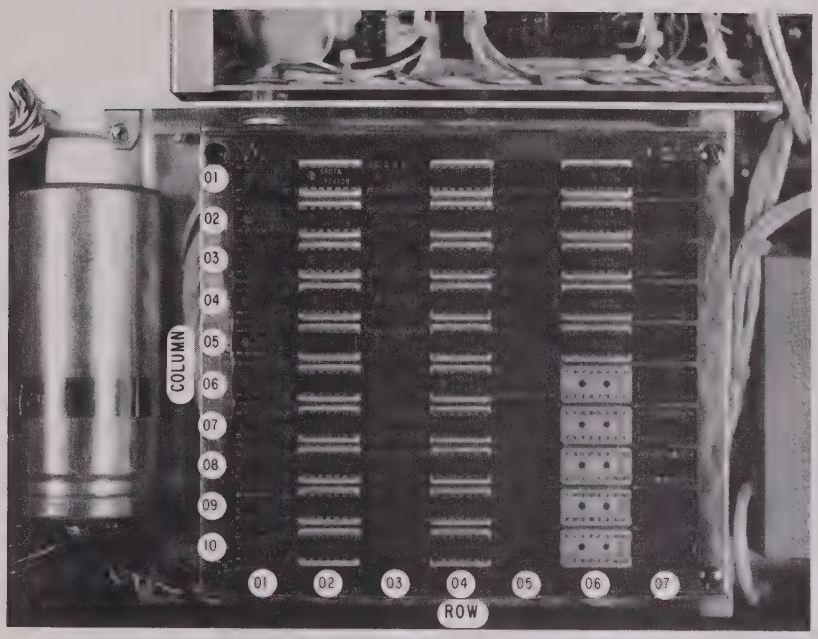
The labels are circuit reference designators corresponding to those used in the circuit diagram figure titles (SECTION V) and the Replacement Parts List (Subsection 6.5).

Figure 6-2 shows the locations of integrated circuits used in the Model 280. Labels correspond to those used in Figure 5-21 and the Replacement Parts List.

6.3.2 Circuit Assembly Removal and Replacement

The correct method of removing circuit assemblies is shown in Figure 6-3.

Grip the card firmly and pull *straight* out. To replace, slide the card into the track, pressing firmly until the top is even with or just below the level of the case.



NOTE: MODULE CIRCUIT REFERENCE DESIGNATORS ARE FORMED

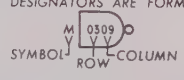
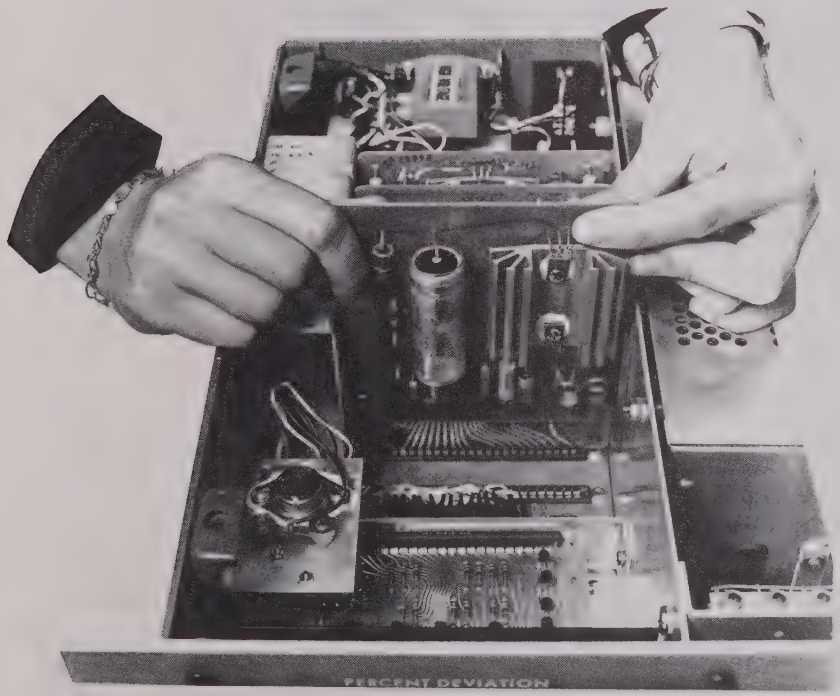


Figure 6-2. Locations of Integrated Circuits



WARNING

Turn power off before removing this assembly (200 V and 5 V Supplies).

Figure 6-3. Removal of Circuit Assembly

6.3.3 Integrated Circuit Removal and Replacement

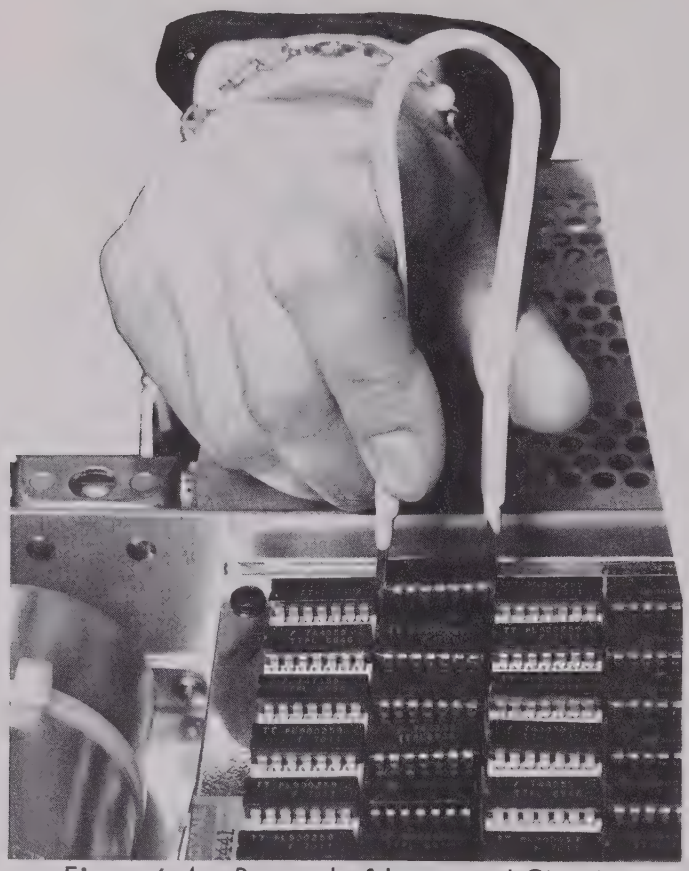


Figure 6-4. Removal of Integrated Circuit

The correct way to remove integrated circuits is shown in Figure 6-4.

Use of a dual in-line extractor (Augat, No. T114-1 shown in the figure above) is strongly recommended. To avoid bending connector pins, grip diagonally opposite corners, brace wrist and lift slowly out. To replace, align the pins carefully and press down evenly, gently at first and then firmly, until the module is evenly seated.

6.3.4 Panel-Mounted Components Removal and Replacement

The only panel-mounted components that might need to be removed are the pushbutton lamps and the display tube assembly.

To remove the display tube assembly, pry off the two vertical bezels, slide the lens out, unscrew the two screws on the lower horizontal bezel and pull the assembly forward. Care must be taken not to hit the tips of the display tubes, as they are rather fragile. (Tubes may be removed before the assembly is unplugged.) Reverse the process to replace.

To remove pushbutton lamps, unscrew and remove the ring nut on the outside of the front panel, then carefully work the switch back through the inside of the unit. It may be necessary to unsolder the wires attached to these switches; in rare cases it may be desirable to remove the capacitor directly behind them for easier access. Reverse the process to replace.

6.4 REPLACING THE COVERS AND CASE

Be sure that the interior of the unit is completely clear of all foreign material. Replace generator and detector covers and the top and bottom covers, tightening all fasteners. Slip the unit onto the metal tracks until you hear a click. Push the unit back into the cabinet, replace all connections previously removed and replace the four mounting screws.

6.5 REPLACEMENT PARTS LIST

The following parts list is in alphanumerical order of the circuit reference designator. Miscellaneous parts are included at the end of the list. Manufacturer of the part is given in a code number according to the Federal Supply Code for Manufacturers (see list of manufacturers below).

Parts manufactured by Electro Scientific Industries must be ordered from the factory. When ordering, include the following information:

Model and serial number of the instrument
Electro Scientific Industries part number
Circuit reference designator
Description of part

CODE LIST OF MANUFACTURERS

01121	ALLEN-BRADLEY COMPANY, Milwaukee, Wisconsin
01295	TEXAS INSTRUMENTS, INC., Dallas, Texas
02735	RCA CORPORATION, Harrison, New Jersey
04713	MOTOROLA CORPORATION, Semi-Conductor Division, Phoenix, Arizona
11837	ELECTRO SCIENTIFIC INDUSTRIES, INC., Portland, Oregon
23095	AZTEC ELECTRONICS, INC., Anaheim, California
56289	SPRAGUE ELECTRIC COMPANY, North Adams, Massachusetts
70903	BELDEN CORPORATION, Chicago, Illinois
72619	DIALIGHT CORPORATION, Brooklyn, New York
75915	LITTELFUSE, INC., Des Plaines, Illinois
83594	BURROUGHS CORPORATION, Plainfield, New Jersey
90201	MALLORY CAPACITOR COMPANY, Indianapolis, Indiana
93790	CORNELL-DUBLIER ELECTRIC CORPORATION, New Bedford, Massachusetts

CKT REF	DESCRIPTION	MFR CODE	MFR PART NUMBER	ESI PART NUMBER	QTY USED	RECM SPARES
A1A1	Circuit Assembly, Detector Preamplifier	11837		20892	1	
A1A2	Circuit Assembly, Detector	11837		20890	1	
A1A3,A2A2,A3A11	Circuit Assembly, Dual 15-volt Regulator	11837		19875	3	
A1A4	Circuit Assembly, 5 V, 250 mA Supply	11837		19883	1	
A1A5	Circuit Assembly, Integrator	11837		20909	1	1
A1A6	Circuit Assembly, Detector Logic	11837		19921	1	
A1T1,A1T2 A3T1,A3T2	Transformer, Pulse	23095	11062	20283	4	
A1T3	Transformer, Power	23095	11130	20902	1	
A2A1	Circuit Assembly, Generator Power Amplifier	11837		19896	1	
A2A3	Circuit Assembly, Voltage Control and Current Limit Relay Driver	11837		19894	1	
A2A4	Circuit Assembly, Generator Reference and Current Limit	11837		19892	1	
A2A5	Circuit Assembly, Generator Buffer Amplifier	11837		20894	1	

CKT REF	DESCRIPTION	MFR CODE	MFR PART NUMBER	ESI PART NUMBER	QTY USED	RECM SPARES
A2C1,A2C2	Capacitor, 600 μF, 75 V	90201	CG62U75A1	13684	2	
A2C3	Capacitor, 0.068 μF, 100 V	93790	WMF-1S68	18841	1	
A2T3	Transformer, Power	23095	11129	20901	1	
A3A4	Circuit Assembly, Digital Display	11837		19870	1	
A3A4M1-M4	Integrated Circuit, Decoder/Driver	01295	SN7441AN	20607	4	2
A3A4V1	Tube, Display, + - Ø	83594	B5448	20862	1	1
A3A4V2-V5	Tube, Display, 0 through 9	83594	B5441	20861	4	2
A3A6	Circuit Assembly, 200 V and 5 V Supplies	11837		19879	1	
A3A7	Circuit Assembly, Logic Interface	11837		19908	1	
A3A8	Circuit Assembly, Lead Check	11837		19890	1	
A3A9	Circuit Assembly, Driver	11837		19928	1	
A3A10	Circuit Assembly, Frequency Source	11837		19904	1	
A3T3	Transformer, Power	23095	11131	20903	1	
C1	Capacitor, 12000 μF, 40 V	56289	36D123G040BC2A	12293	1	
DS1	Pushbutton Lamp, Clear, MEASURE	72619	913-1153-1635-525	20277	1	1
DS2	Pushbutton Lamp, Amber, RESET	72619	913-1153-1633-525	20275	1	1
DS3	Pushbutton Lamp, Red, LEAD FAIL	72619	913-1153-1631-525	20276	1	1
F1	Fuse, 1.5 A, 125 V	75915	31201.5	20280	1	
M0101,0506,0507	Integrated Circuit	01295	SN7430N	20605	3	1
M0102,0201,0304, 0406	Integrated Circuit	01295	SN7440N	20606	4	2
M0103,0204,0206, 0207,0309,0310	Integrated Circuit	01295	SN7473N	20613	6	2
M0104-0106,0109, 0202,0203,0208, 0210,0301-0304, 0306,0307,0405, 0505,0509,0510, 0709	Integrated Circuit	01295	SN7400N	20600	19	4
M0107,0108,0110, 0209,0308,0407-0410,0508	Integrated Circuit	01295	SN7420N	20604	10	3
M0205,0501-0504	Integrated Circuit	04713	MC858P	20627	5	2
M0401-0404	Integrated Circuit	01295	SN7490N	20616	4	2
M0601-0605	Integrated Circuit	01295	SN7475N	20614	5	2
M0710	Integrated Circuit	04713	MC830P	20620	1	1
Q1	Transistor	02735	2N3055	13589	1	
S3	Switch, MODE	11837		19948	1	
	Cap, Binding Post, Black	11837		1476	9	
	Cap, Binding Post, Gold	11837		1172	2	
	Fuse Holder	75915	342012	3074	1	
	Knob, Small Bar	11837		1473	1	
	Knob, Large Bar	11837		1458	2	
	Manual, Maintenance	11837		19859	1	
	Power Cord	70903	17258-B	13178	1	

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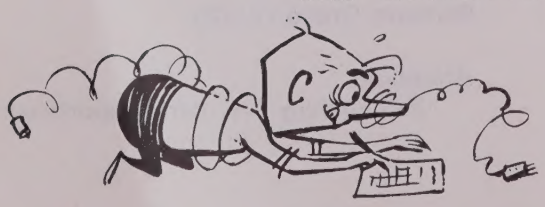

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